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INTERFACE AND INSTALLATION MANUAL

DIGITAL EQUIPMENT CORPORATION • MAYNARD, MASSACHUSETTS

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PDP-7 INTERFACE AND INSTALLATION MANUAL

DIGITAL EQUIPMENT CORPORATION • MAYNARD, MASSACHUSETTS

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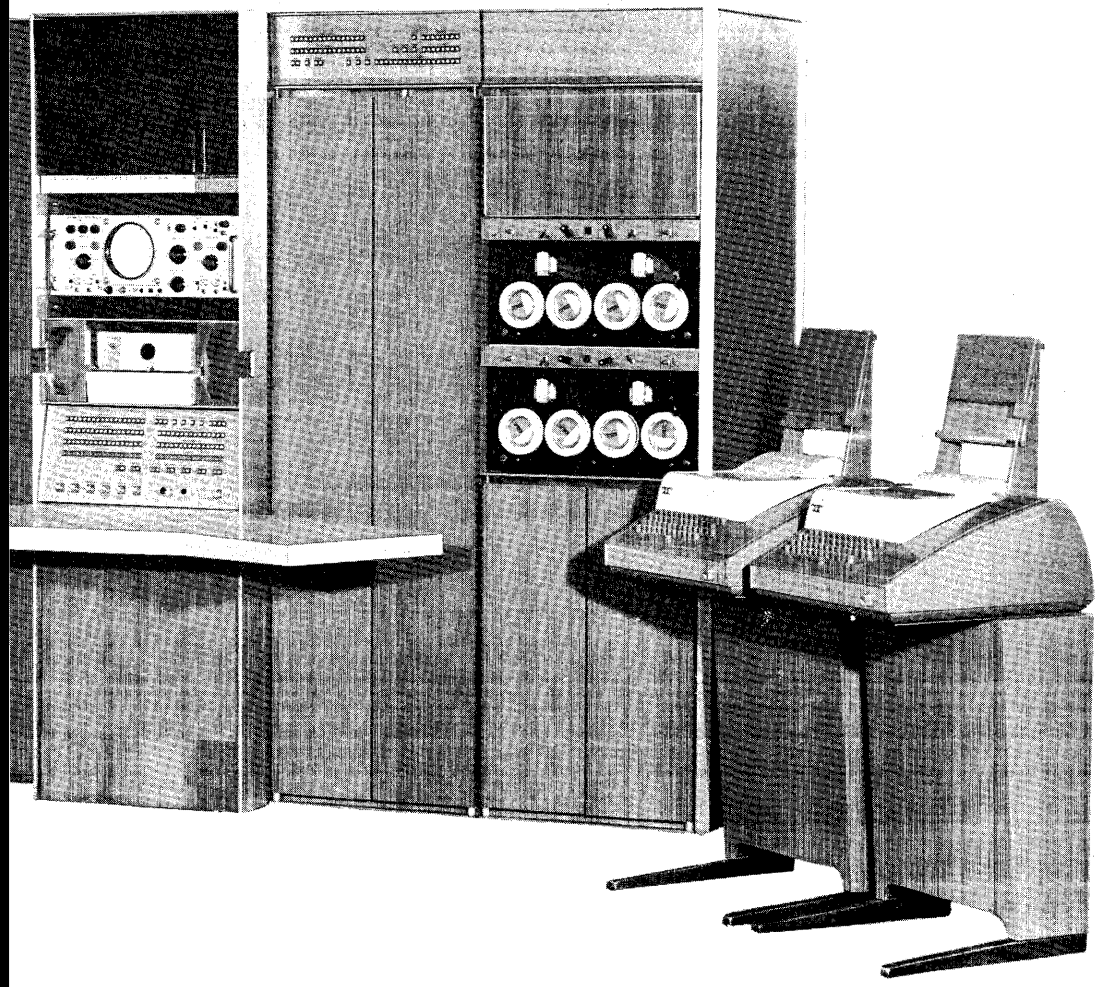

Typical PDP-7 Installation

CHAPTER 1

INTRODUCTION

Since the processing power of a computer system depends, in large measure, upon the range and number of peripheral devices that can be connected to it, the Programmed Data Processor-7 (PDP-7) has been designed with a very broad, flexible, and expandable interface. This manual defines the interface characteristics of the computer to allow the reader to design and implement any electrical interfaces required to connect devices to the PDP-7. This manual also provides information for planning the installation of a PDP-7 system. Information in this manual applies only to PDP-7 systems with serial numbers above 100. Refer to the PDP-7 Interface and Installation Manual, F-78, dated 1/66, for information on systems with serial numbers below 100.

The PDP-7 is a digital machine designed for use as a general-purpose computer, an independent information handling facility, or as the control element in a complex processing system. The PDP-7 is a single-address, fixed 18-bit word length, parallel processing binary computer using 1's complement arithmetic (2's complement arithmetic facilitates multiprecision operations). Cycle time of the random-access core memory is 1.75 μsec, permitting a computation rate of up to 285,714 additions per second.

Programming features of the computer include indirect addressing, microprogramming (combining instructions to occur in one 1.75-μsec machine cycle), and programmed monitoring of peripheral devices. Real-time features of the computer include program interrupt (entry into a subroutine caused by a request from an I/O device), input/output skip facility (program flow modification as a function of the status of a selected peripheral device), and high-speed data break channel (direct input/output access to computer core memory for cycle-stealing data transfers at a rate of over 10 million bits per second). Eight autoindex registers simplify sorting, searching, and multiple input/output list processing operations. An operator console provides manual control and visual indication of programmed operations. An 18-bit switch register permits manual entry of data and instructions, or status information to be sensed by the program. The console displays all active registers, including the memory address register, memory buffer register, accumulator, link bit, machine state, instruction register, program counter register, and multiplier quotient register of the optional extended arithmetic element.

The basic PDP-7 system consists of a Type KA77A Processor, a Type 149 Core Memory, and a Type KA71A I/O Package composed of FLIP CHIP™ circuit modules and solid-state power supplies. These hybrid silicon

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circuits have an operating temperature range exceeding the limits of 32° to 122°F, so no air-conditioning is required at the computer site. Standard 115v, 60-cps power operates the computer. The basic system is self-contained in a 3-bay cabinet 69-1/8 inches high and 61-3/4 inches wide. This unit weighs approximately 1150 lb, requiring no subflooring or bracing.

In addition to the standard tape reader, tape punch, and Teletype keyboard/reader, the PDP-7 system can operate over 64 input/output devices. Existing interface designs permit connection of a number of DEC options to the computer, including devices such as line printers, magnetic tape transports, magnetic drums, card equipment, analog-to-digital converters, CRT displays, and digital plotters. The PDP-7 system can also accept other types of instruments or hardware devices that have an appropriate interface. The simple I/O techniques of the PDP-7 allow inexpensive, straight-forward device interfaces to be realized. Any device interface needs control to determine when an information exchange is to take place and to specify the location(s) in the computer core memory which accept or yield data. Either the computer program or the transferring device may exercise this control. Transfers made under control of the computer program are called programmed data transfers. Transfers made under control of the external device are called data break transfers.

PROGRAMMED DATA TRANSFERS

The majority of I/O transfers occur under control of the computer program. The maximum realistic rate of transferring 18-bit words is 33 kc in the program interrupt mode. Normally this speed is well beyond that required for laboratory or process control instrumentation. To transfer and store information under program control requires about six times as much computer time as under data break control. In terms of real time, the duration of a programmed transfer is rather small due to the high speed of the computer.

To realize full benefit of the built-in control features of the PDP-7 programmed I/O transfers should be used in most cases. Controls for devices using programmed data transfers are usually simpler and less expensive than controls for devices using data break transfers. Analog-to-digital converters, digital-to-analog converters, digital plotters, line printers, message switching equipment, and relay control systems typify equipment using the programmed data transfer channels.

Using programmed data transfer channels, simultaneous operation of devices is limited only by the relative speed of the computer with respect to the device speeds, and the search time required to determine the device requiring service. The percent of computer time taken for I/O servicing is roughly:

$$\%\text{I/O time} = \text{sum of device rates (in cps)} \times \text{service time (}\mu\text{sec per interrupt)} \times 10^{-4}$$

For comparison, it takes less than 3% of computer running time to read or write conventional IBM-compatible magnetic tape at 556 bits per inch and 75 inches per second.

DATA BREAK TRANSFERS

Devices which operate at very high speed or which require very rapid response from the computer use the data break transfer channel. This channel permits an external device, almost arbitrarily, to insert or extract words from the computer core memory, bypassing all program control logic. Because the computer program has no cognizance of transfers made through this channel, programmed checks of input data are made prior to use of information received in this manner.

The data break is particularly well-suited for devices that transfer large amounts of data in block form, e.g., high-speed magnetic tape systems, high-speed drum memories, or CRT display systems containing memory elements.

PERTINENT DOCUMENTS

The following publications serve as source material and complement the information in this manual.

1. Digital Logic Handbook, C-105. This book describes the functions and specifications of FLIP CHIP modules and module accessories used in the PDP-7, control interfaces, and peripheral devices.

2. PDP-7 Brochure, F-71. This leaflet presents the basic functions of the PDP-7 hardware, software, instructions, and standard optional equipment.

3. PDP-7 Users Handbook, F-75. This book contains computer organization information, detailed information on the function of interface facilities, and descriptions of the timing and operations performed by all instructions.

4. PDP-7 Maintenance Manual, F-77A. This manual gives functional description, principles of equipment operation, interface, installation, operating procedures, and detailed maintenance information for machines with serial numbers above 100.

5. Instruction manuals for appropriate input/output device options used in PDP-7 systems are available.

6. PDP-7 Price List, F-72. This leaflet contains current price information on the basic computer, computer options, and standard input/output equipment.

LOGIC SYMBOLS

Figure 2 defines the symbols used to express digital logic circuits and signals in the illustrations of this manual.

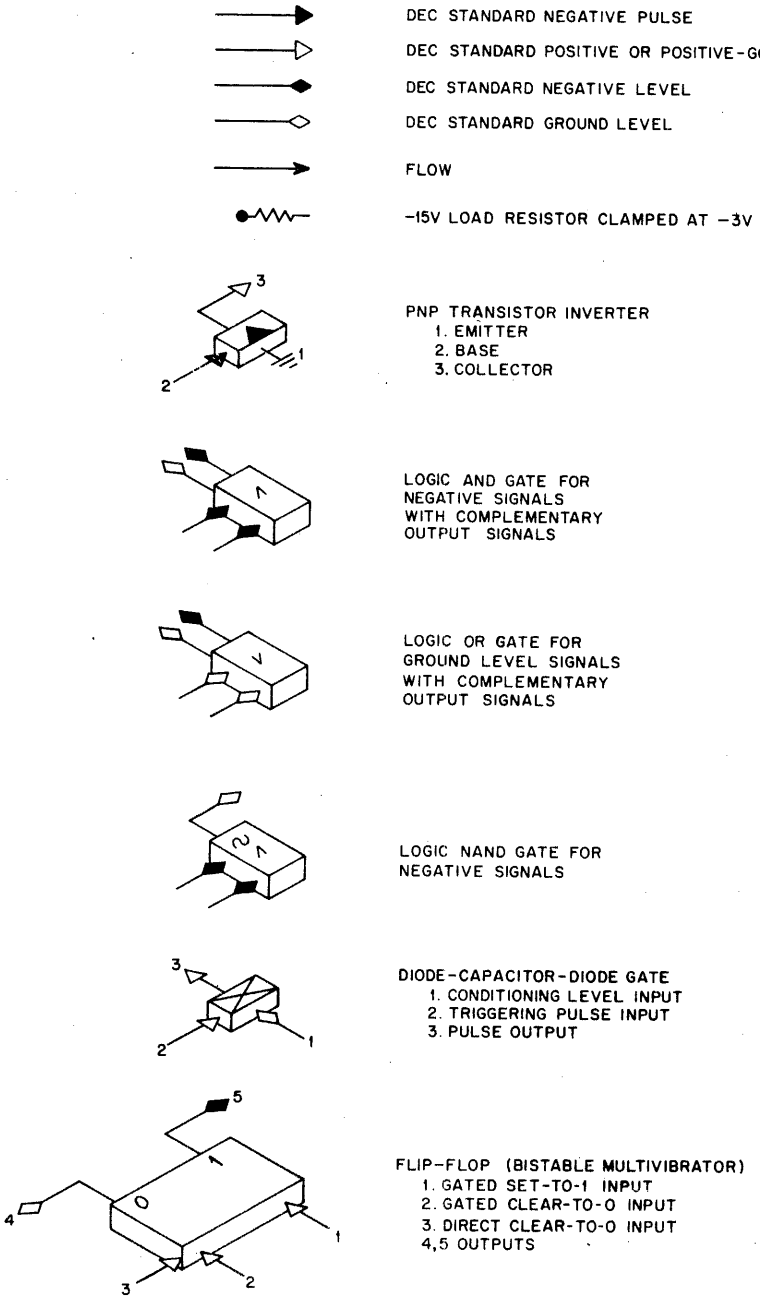


Figure 2 Logic Symbols

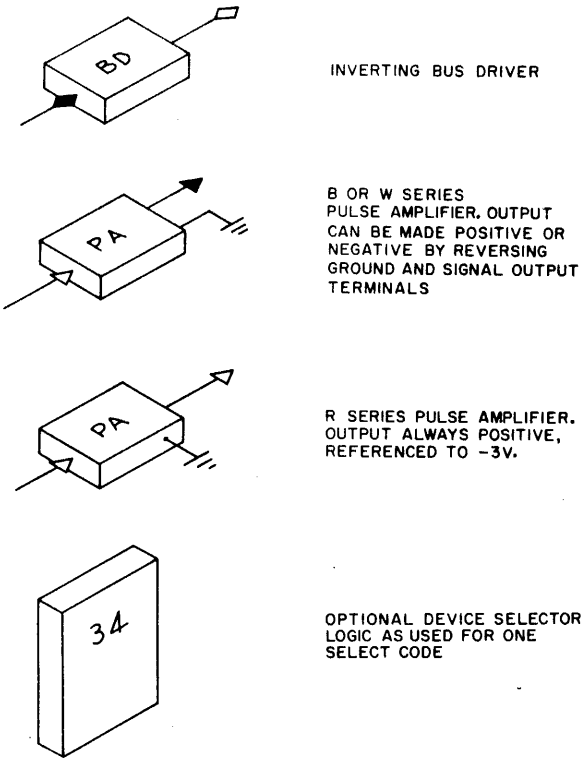


Figure 2 Logic Symbols (continued)

CHAPTER 2

PROGRAMMED DATA TRANSFERS

The PDP-7 is a parallel-transfer machine that collects and distributes data in bytes of up to 18 bits. Figure 3 shows information flow within the computer to effect a programmed data transfer with input/output equipment.

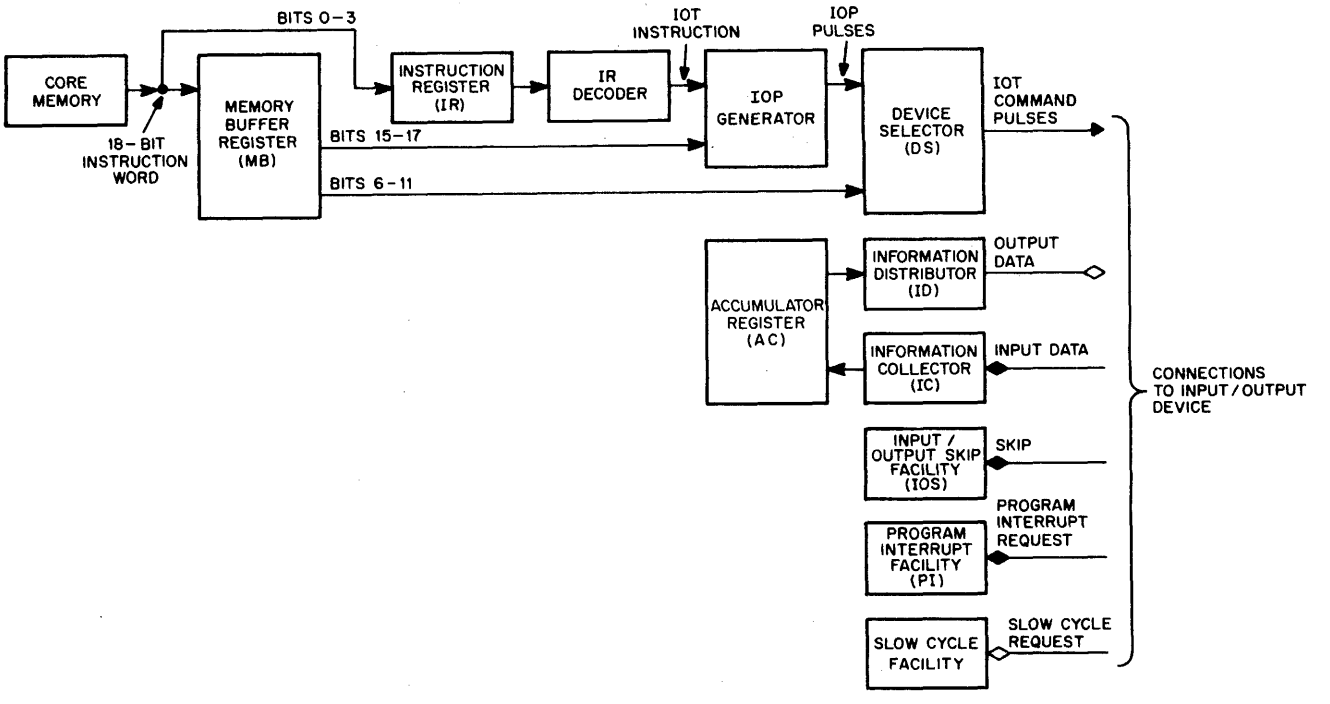


Figure 3 Programmed Data Transfer Interface Block Diagram

All programmed data transfers take place through the accumulator, the 18-bit arithmetic register of the computer. The computer program controls the loading of information into the accumulator (AC) for an output transfer, and for storing information in core memory from the AC for an input transfer. Information in the AC for output transfer is power amplified and supplied to the bussed connections of many peripheral devices by the information distributor (ID). Then the program-selected device can sample these signal lines to strobe AC data into a control or information register. Input data signals arrive from many peripheral devices at input mixer circuits of the information collector (IC), which transfers data into the AC. In the input/output skip facility (IOS), command pulses from the device selector (DS) sample the condition of I/O device flags. The IOS allows branching of the program based on the condition or availability

of peripheral equipment, effectively making programmed decisions to continue the current program or to jump to another part of the program, such as a subroutine that services an I/O device.

The DS generates command pulses during execution of input/output transfer (IOT) instructions. All instructions stored in core memory as a program sequence are read into the memory buffer register (MB) to be executed. The operation code in the four most significant bits (bits 0 through 3) of the instruction is transferred into the instruction register (IR) and decoded to produce appropriate control signals. When the operation code is recognized as an IOT instruction, the IOP generator produces time-sequenced IOP pulses as a function of the three least significant bits of the instruction (bits 15 through 17 in the MB). The IOP pulses, with an I/O device selection code in bits 6 through 11 of the instruction, are supplied as bus inputs to all gates of the DS. The gating circuits of the DS associated with a specific device are enabled by the select code to regenerate IOPs as specific IOT command pulses. Figure 4 shows the decoding of an IOT instruction and Figure 5 indicates the timing of the IOP and IOT pulses.

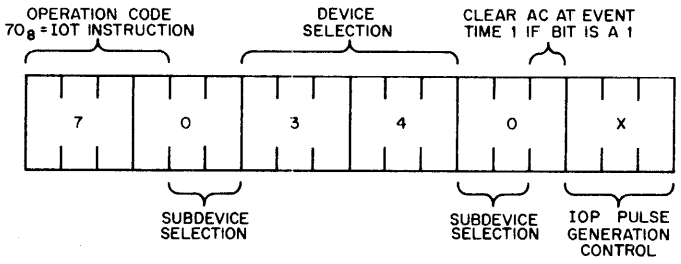
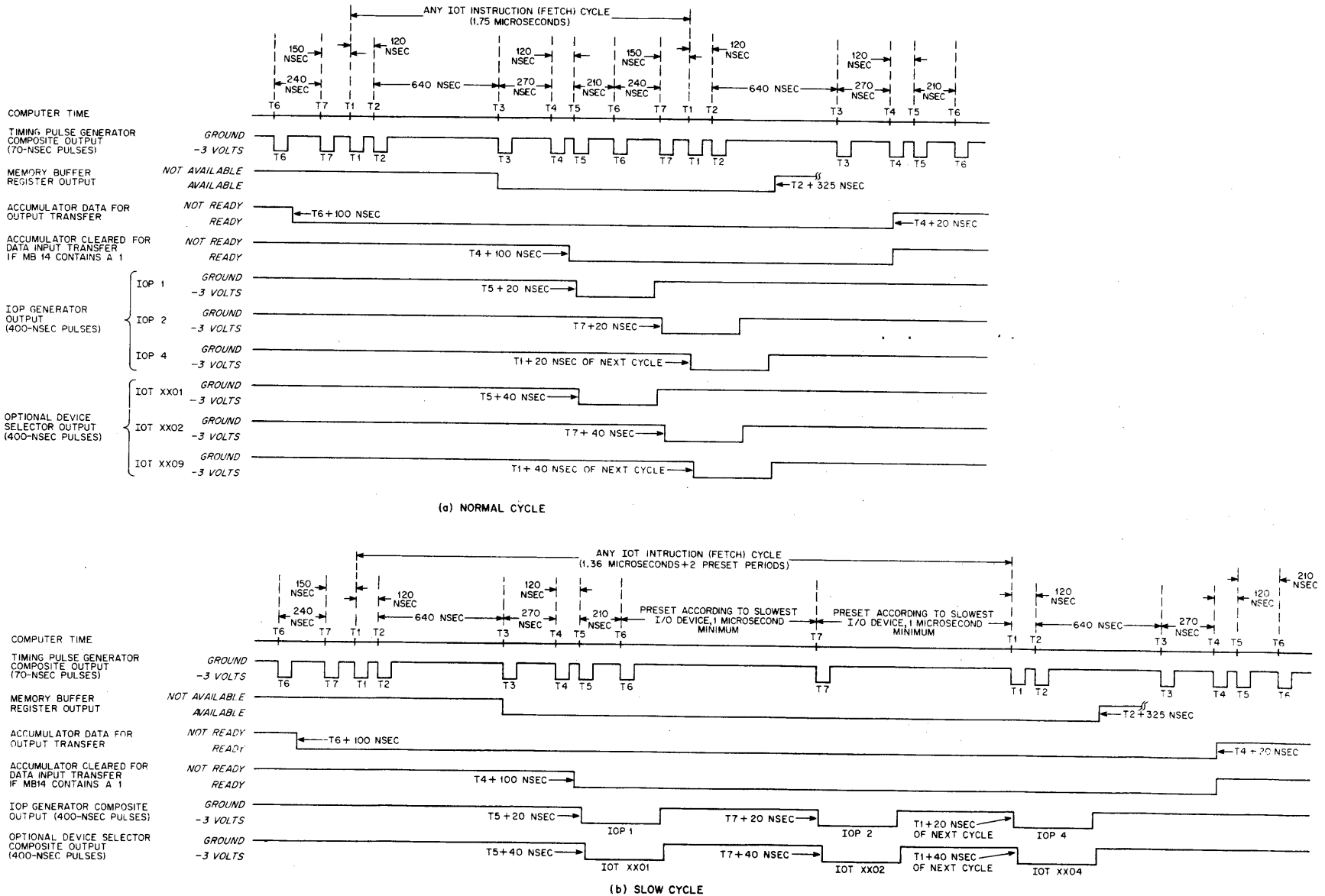


Figure 4 Decoding of IOT Instructions

One IOT instruction can generate one, two, or three sequential IOT pulses. These command pulses are designated by the octal code of the twelve least significant bits of the instruction in which they are generated; e.g., IOT 3401 (usually bits 4 and 5 are unused and are assumed to be 0's unless otherwise specified). These IOT command pulses from the DS go to the IOS, the IC, and to a specific I/O device whose action they control. In this manner, the program produces commands to transfer data into or out of I/O devices; to cause the program to skip or not skip an instruction based on the condition of an external device flag; or to start, stop, or perform operations in devices controlled by a command pulse.

IOT instructions can use the normal computer cycle time of 1.75 μsec, or can occur in a slow cycle adjusted to the speed of the slowest I/O device. The device selector can be wired to cause entry into a slow cycle for any device, when its select code is in the IOT instruction being executed. Figure 5 shows the timing of command pulses for devices using the normal or slow cycle and the availability of the AC for transfers.



(a) NORMAL CYCLE

(b) SLOW CYCLE

Figure 5 Programmed Data Transfer Timing Diagram

Devices which require immediate service from the computer program, or which take considerable computer time to discontinue the main program until transfer needs are met, can use the program interrupt (PI) facility. In this mode of operation, the computer can initiate operation of I/O equipment and continue the main program until the device requests servicing. A signal input to the PI requesting a program interrupt causes storing of the conditions of the main program and initiates a subroutine to service the device. At the conclusion of this subroutine, the main program is reinstated until another interrupt request occurs.

TIMING CYCLE

Cycle time of an IOT instruction is either normal or slow, depending upon the device addressed (see Figure 5). All devices use the normal cycle unless the device selector for the selected equipment is wired to request a slow cycle.

The normal IOT cycle time is 1.75 μsec, or equal to a normal computer cycle. At computer time 5 (T5) IOP1 is produced, at time 7 (T7) IOP2 is produced, and at time 1 (T1) of the next cycle IOP4 is produced. Time 1 of the next cycle can be used for IOP4, since time 1 is normally used only to prepare to read the next instruction into the MB from core memory; so the IR and MB still contain the same information. The time from the start of IOP1 to the start of IOP2 is 450 nsec; from the start of IOP2 to IOP4 is 150 nsec. If consecutive IOT instructions occur, the time from the start of IOP4 in the first instruction to the start of IOP1 of the second instruction is 1.15 μsec.

The slow IOT cycle time produces IOP pulses at the same computer times as during a normal cycle; however, the delay between timing pulses is adjustable from a 1 μsec to 4 μsec. Under special conditions modifications to the delay modules can produce even longer time delays. In all cases, delays are set to accommodate the slowest device using the slow cycle feature of the computer (this timing exists for all devices requesting a slow cycle). A complete slow cycle requires a 3.36 μsec minimum.

IOP GENERATOR

The logic circuits of the IOP generator are shown in Figure 6. When the instruction register decoder detects an IOT instruction (the operation code in bits MB0-MB5 = 1110_2), it generates the IOT signal. The IOT signal conditions one input of each of the three gates that trigger pulse amplifiers to produce the IOP pulses. Each 3-input NAND gate is operated by the condition of a bit in the IOT instruction and a computer timing pulse, to produce one of the sequential IOP pulses. Each IOP pulse goes to one gate of all device selector channels to allow generation of an IOT command pulse at one of the three sequential event times within the instruction. Figure 6 shows the computer timing pulses and instruction bit conditions which generate each IOP pulse for the three event times.

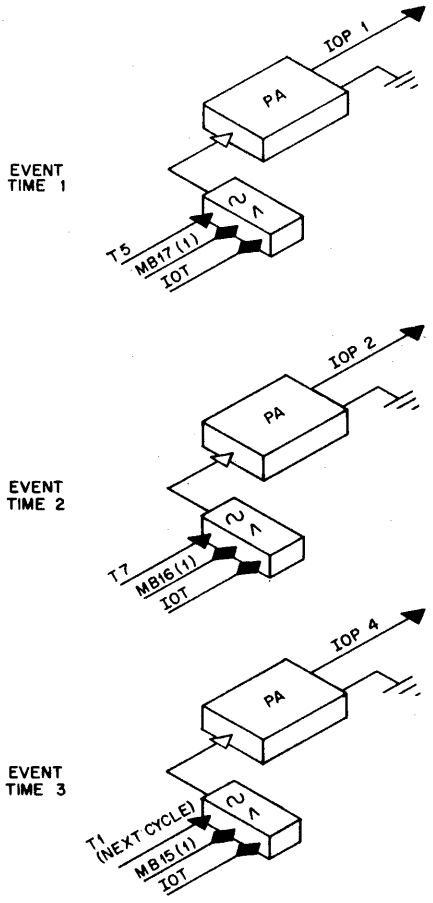


Figure 6 IOP Generator

DEVICE SELECTOR (DS)

The DS selects an I/O device or subdevice according to the address code of the device specified in bits 4 through 13 of the IOT instruction. Selection of the device can request a slow cycle. The DS then generates IOT command pulses for each IOP pulse received, and transmits these commands to the IOS, the IC, and/or the device. Generally, IOT command pulses are used as follows:

Command	Use
IOT XX01	Applied to the IOS to sense the condition of the device flag.
IOT XX02	Applied to the IC to transfer data into the computer, or applied to the device to initiate a data transfer from the computer and clear device flags.
IOT XX04	Applied to the device to initiate some operation (start, read, etc.).

Each group of these command pulses requires one channel of the DS, and each channel requires a different address (or select code). One device can, therefore, use several channels of the DS. Figure 7 shows generation of command pulses by several channels of the DS.

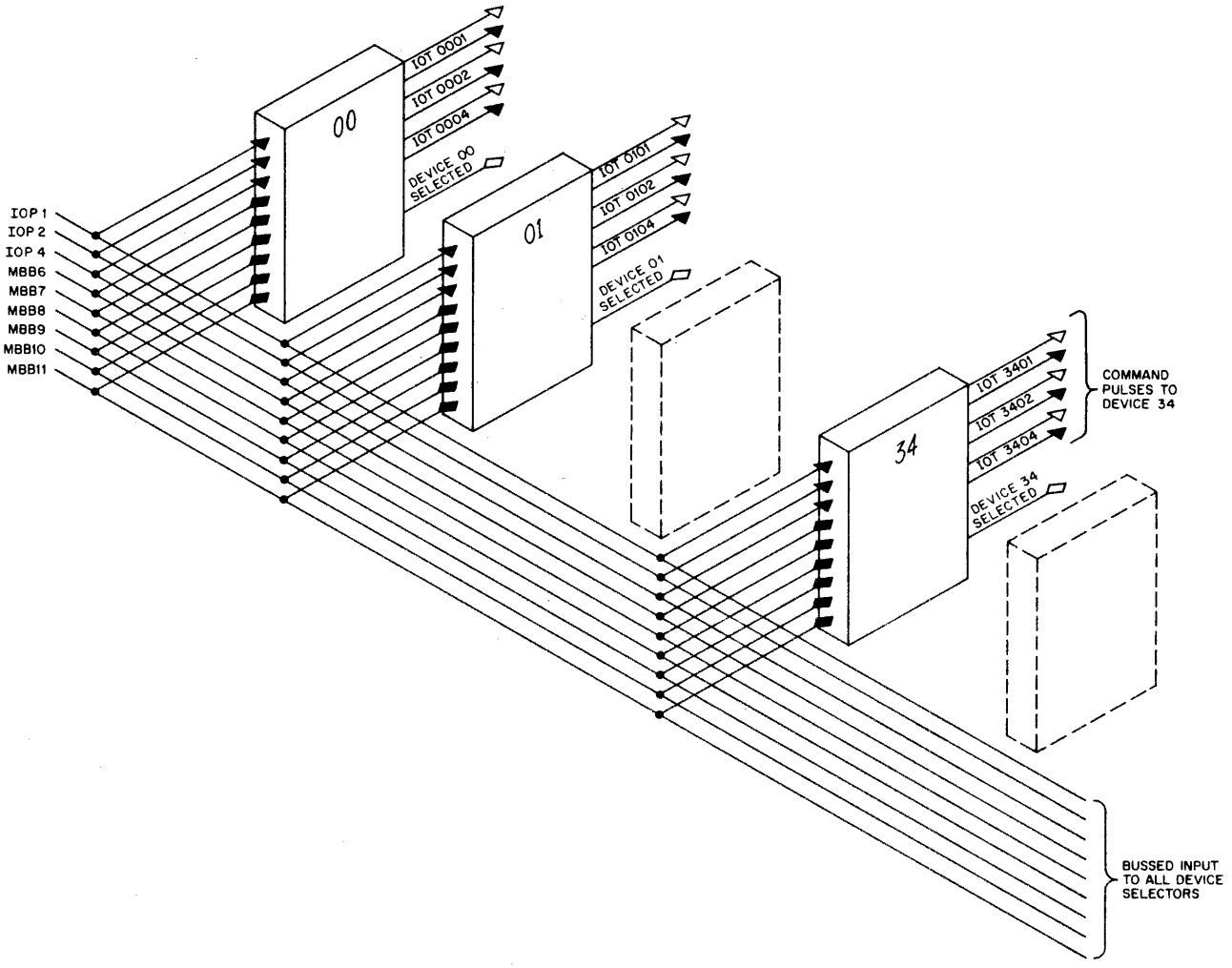


Figure 7 Generation of IOT Command Pulses by Device Selector

The logical representation for a typical channel of the DS, using channel 34, is shown in Figure 8. A 6-input NAND gate wired to receive the appropriate signal outputs from MB6-11 for select code 34 activates the channel. In the DS module, the NAND gate contains 14 diode input terminals; 12 of these connect to the complementary outputs of MB6-11, and 2 are open to receive subdevice or control condition signals as needed. Either the 1 or the 0 signal from each MB bit is disconnected by removing the appropriate diode from the NAND gate when establishing the select code. The ground level output of the NAND gate indicates when the IOT instruction selects the device, and can therefore request a slow cycle

for the device. This output also enables three gating inverters, allowing them to trigger a pulse amplifier if an IOP pulse occurs. The positive output from each pulse amplifier is an IOT command pulse identified by the select code and the number of the initiating IOP pulse. Three inverters receive the positive IOT pulses to produce complementary IOT output pulses. A pulse amplifier module can be connected in each channel of the DS to provide greater output drive or to produce pulses of a specific duration required by the selected device.

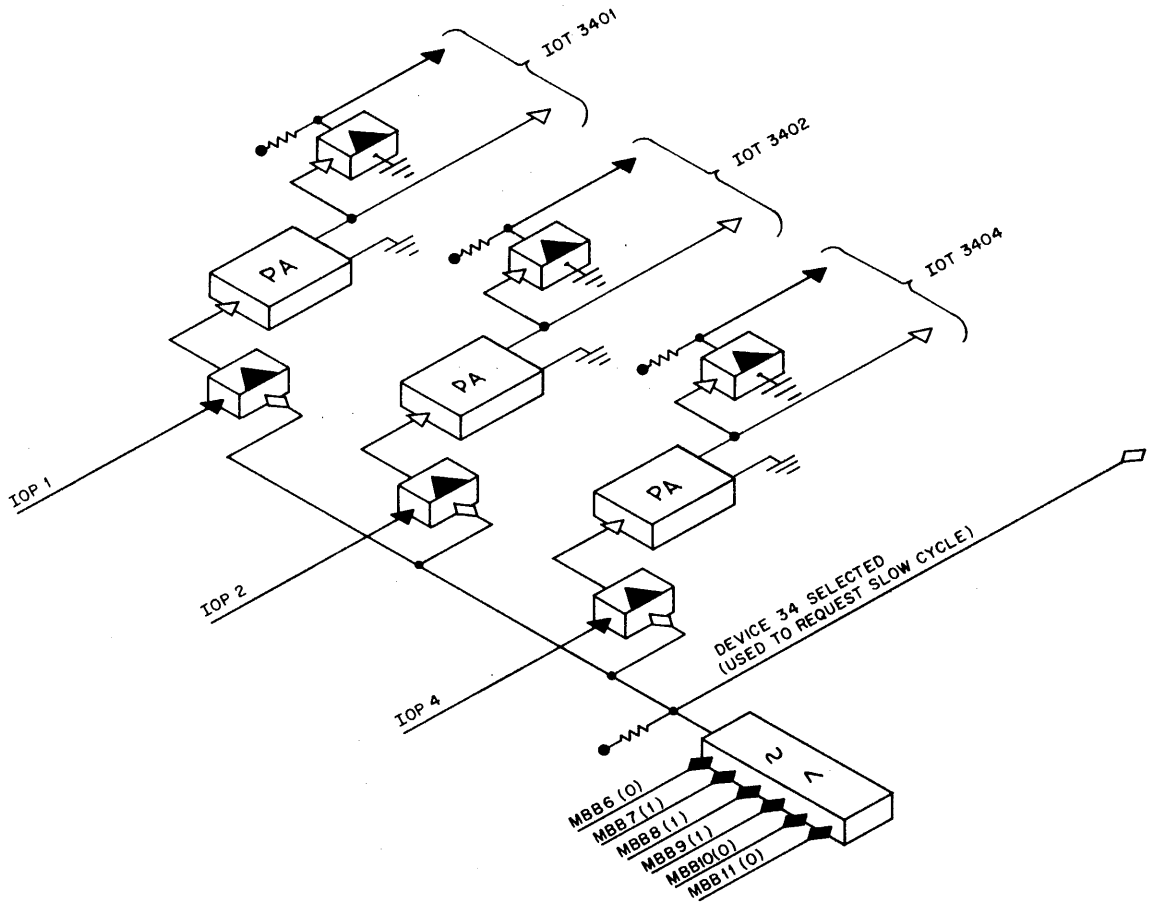


Figure 8 Typical Device Selector (Device 34)

SLOW CYCLE FACILITY

Up to twelve devices can request a slow IOT cycle by connecting the ground-level select signal output of the DS channel to the slow cycle request facility. This facility consists of a 12-input diode NOR gate for ground levels as shown in Figure 9. None of the basic PDP-7 input/output devices require a slow cycle.

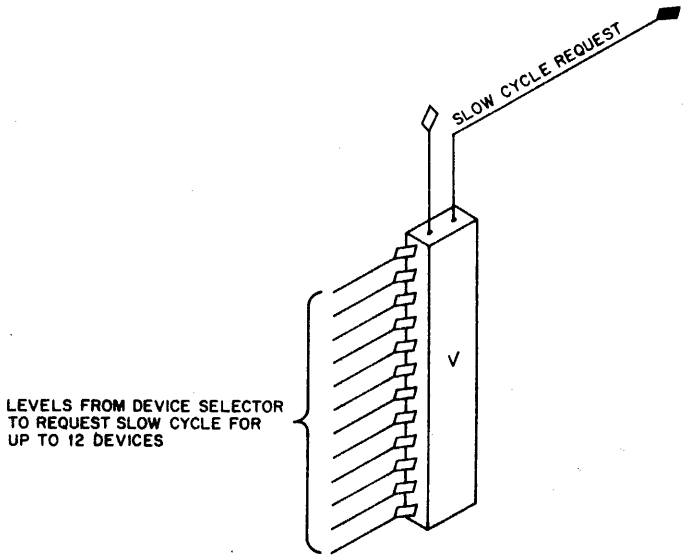


Figure 9 Slow Cycle Facility

INPUT/OUTPUT SKIP (IOS)

The condition of an I/O device flag and generation of an IOT pulse combine in the IOS to cause the program to skip over one instruction. Incrementing the program count without executing the instruction at the current program count causes skipping. The IOS facility consists of multiple 2-input AND gates with outputs connected in parallel to allow any gate to trigger the pulse amplifier which produces the IO SKIP pulse. A flag or status level from the device and an IOT XX01 pulse from the appropriate channel of the DS provide input connections to each gate as shown in Figure 10. In this manner an IOT instruction can check the status of an I/O device and skip the next instruction if the device requires servicing. Programmed testing in this manner allows the routine to jump out of a sequence to a subroutine that services the device tested.

Assuming that a device is already operating, a possible program sequence to test its availability follows:

Address	Instruction	Remarks
⋮		
100,	703401	/SKIP IF DEVICE 34 IS READY
101,	600100	/JUMP .-1
102,	10XXXX	/ENTER SERVICE ROUTINE FOR DEVICE 34
⋮		

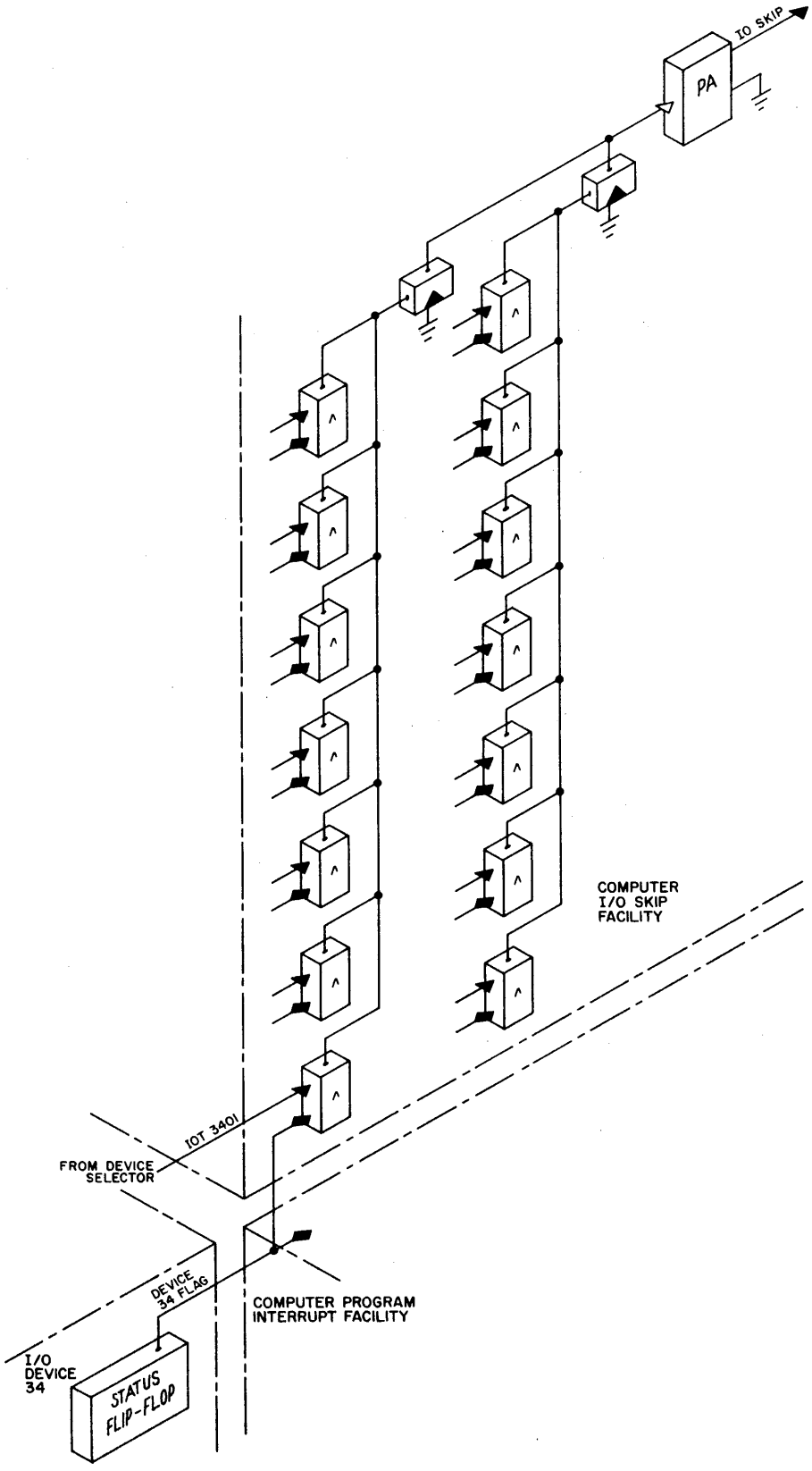


Figure 10 Input/Output Skip Facility

When the program reaches address 100, it executes an instruction skip with 703401. The skip occurs only if device 34 is ready when the IOT 3401 command is given. If device 34 is not ready, the flag signal disqualifies the IOS gate, and the skip does not occur. Therefore, the program continues to the next instruction which is a jump back to the skip instruction. In this example, the program stays in this waiting loop until the device is ready to transfer data, at which time the gate in the IOS is enabled and the skip occurs. When the skip occurs, the instruction in location 102 transfers program control to a subroutine to service device 34. This subroutine can load the AC with data and transfer it to device 34, or can load the AC from a register in device 34 and store it in some known core memory address.

INFORMATION COLLECTOR (IC)

The information collector is a 7-channel gated input mixer that transfers bytes of up to 18 bits into the AC from signals supplied by an external device. Each channel consists of 18 2-input diode AND gates, triggered by a common IOT command pulse from the DS. (Usually the IOT instruction that strobes information into the AC via the IC is microprogrammed with bit 14 containing a 1 so that the AC is cleared at event time 1.) Figure 11 shows the IC logic circuit configuration.

The perforated tape reader and I/O status bits each occupy one 18-bit IC channel. The teleprinter occupies eight bits of a third channel. The remaining four and one-half channels are available for connection to any peripheral and optional input equipment. Each PDP-7 input option connects directly into one or more channels of the IC. For operation of more than seven input devices, the IC is easily expandable in blocks of seven channels to accommodate any number of channels.

INFORMATION DISTRIBUTOR (ID)

The ID is an output bus system that transfers information from the AC to external devices. Accumulator output signals are buffered by 18 bus driver circuits and driven through cables to the I/O package. The ID in the I/O package contains nine 18-bit connection points, or channels, for each bussed signal; one channel receives bussed connections from the processor, seven channels are available for individual device cable connections, and one channel is for external expansion of the ID. (The paper tape punch and teleprinter receive AC output signals directly from the bus drivers and do not require connection through the ID.) If all seven channels are used, the ID can be expanded to any number of output channels by adding suitable non-inverting buffering and distribution channels similar to the standard ID.

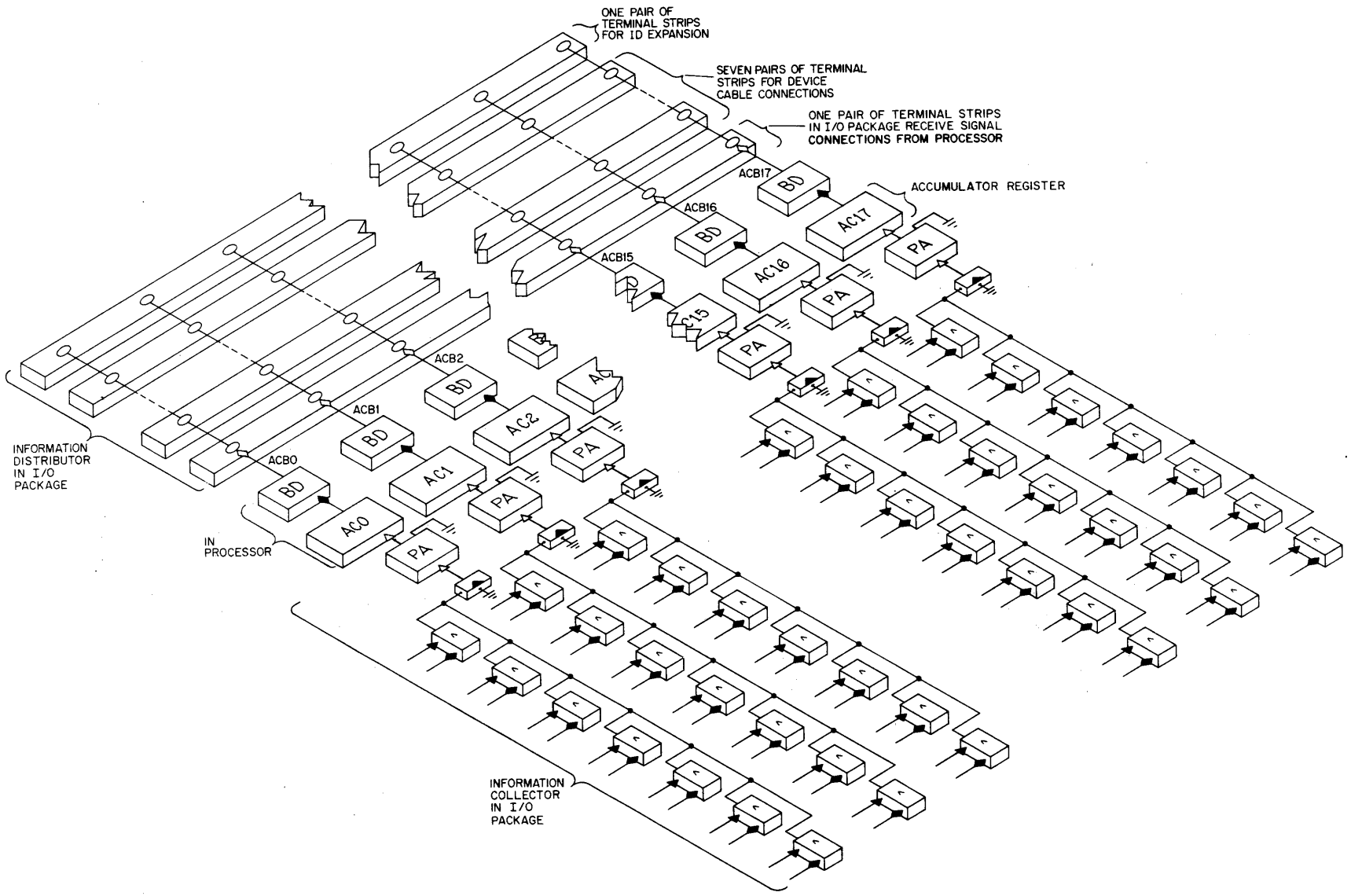


Figure 11 Information Collector and Information Distributor

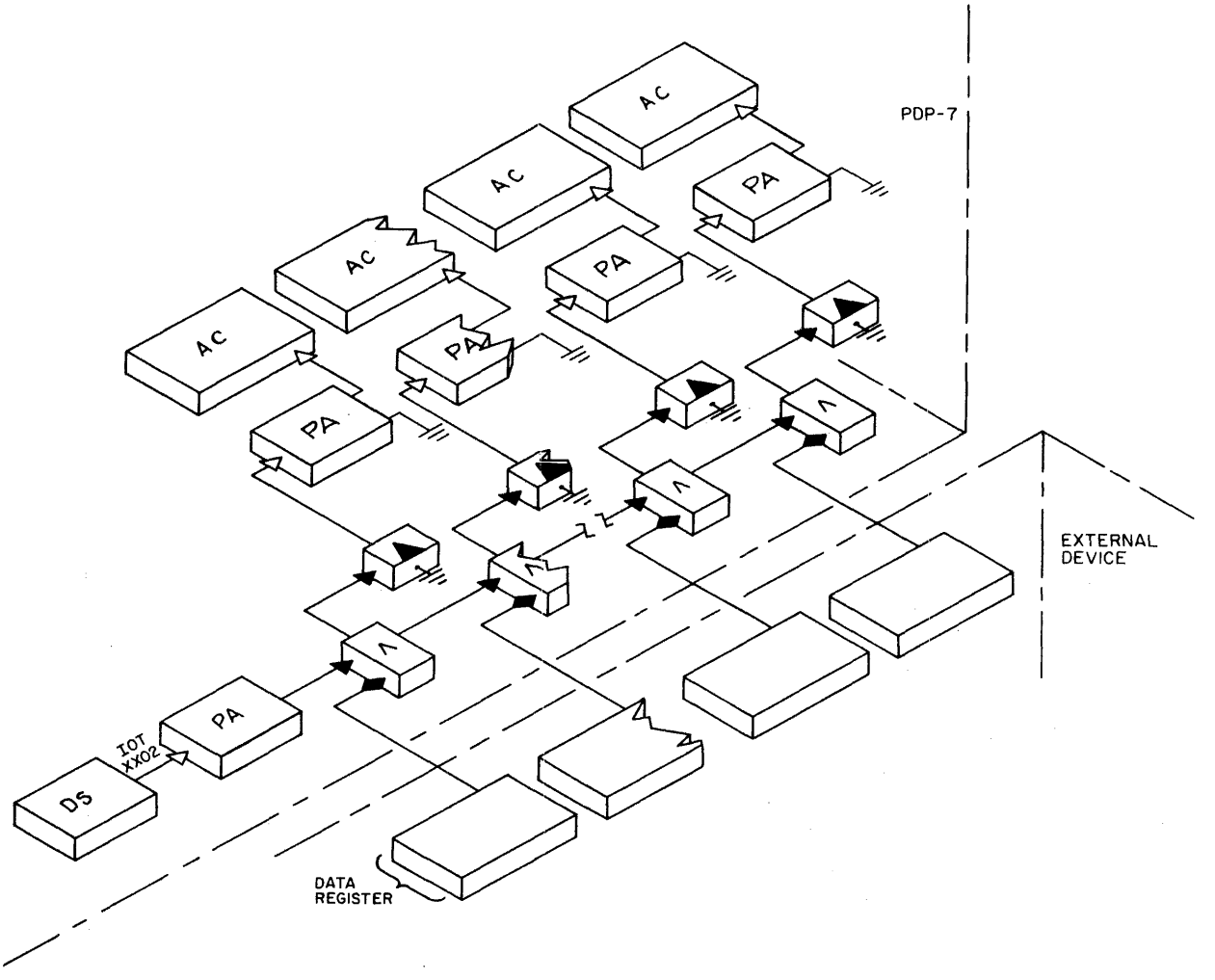


Figure 12 Programmed Data Input Transfer

DATA TRANSFERS INTO THE PDP-7

IOT XX02 and IOT XX04 command pulses control an external input device as indicated in Figure 12. When ready to transfer data into the PDP-7 accumulator, the device sets a flag connected to the IOS. The program senses the ready status of the flag and issues an IOT instruction to read the contents of the external device buffer register into the AC. Usually this instruction contains a clear AC command and an IOT XX02 (IOT XX12) to effect the transfer. If the AC is not cleared before the transfer, the resultant word in the AC is the inclusive OR of the previous word in the AC and the word transferred from the device buffer register. To clear the AC prior to the transfer, bit 14 of the IOT instruction should contain a 1. This microprogramming clears the AC at event time 1 (computer time T5), and an IOT XX12 pulse causes the transfer to occur at event time 2 (computer time T7).

Following the transfer (possibly in the same instruction) the program issues an IOT XX04 command pulse to initiate further operation of the device. This pulse also clears the device flag. For simplicity, the transfer path in Figure 12 shows only a single channel of the IC gates.

DATA TRANSFERS OUT OF THE PDP-7

IOT XX02 and IOT XX04 command pulses control an external output device as indicated in Figure 13. The AC is loaded with a word (e.g., by a LAC instruction); then the IOT instruction is issued to transfer the word into the control or data register of the device by an IOT XX02 pulse, and operation of the device is initiated by an IOT XX04 pulse. The word transferred in this manner can be a character to be operated upon, or can be a control word sampled by a status register to establish a control mode.

Connecting an output device to the PDP-7 interface adds at least three commands to the instruction repertoire. These commands use an IOT XX01 pulse to skip on the ready condition of the device flag, an IOT XX02 pulse to effect a transfer from the AC to the device, and an IOT XX04 pulse to initiate operation of the device.

PROGRAM INTERRUPT (PI)

When a large amount of computing is required, the computer should process data rather than simply wait for an I/O device to become ready to transfer data. The PI facility, when enabled by the program, relieves the main program of the need for repeated flag checks by allowing I/O device ready flags to automatically cause a program interrupt break. At the break location, program control transfers to a subroutine which determines the requesting device and initiates an appropriate service routine.

The basic PI facility can accommodate interrupt requests from nine devices and is expandable. As shown in Figure 14, the PI facility receives a negative signal from the flag of a device to request an interrupt.

This flag signal input to the PI can also connect to the IOS facility to allow the program interrupt subroutine to detect the device requesting the interrupt if multiple devices are connected to the PI. On Figure 14, note that any flip-flop or flag signal connected to an input of any of the six 3-input NOR gates of the I/O package triggers the interrupt control circuits of the processor to cause a program interrupt break, (if a break is not already in progress and if the interrupt system is enabled).

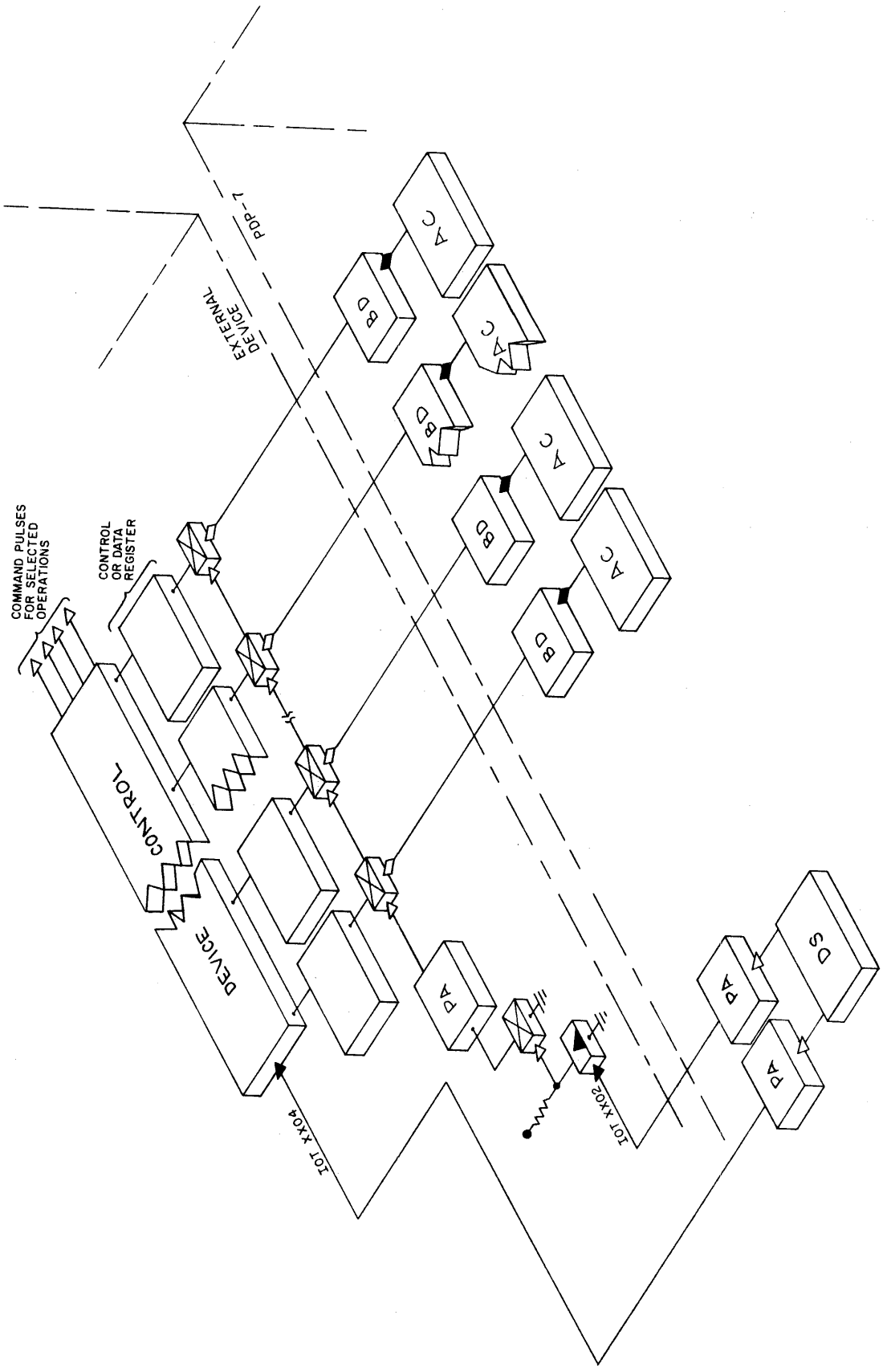


Figure 13 Programmed Data Output Transfer

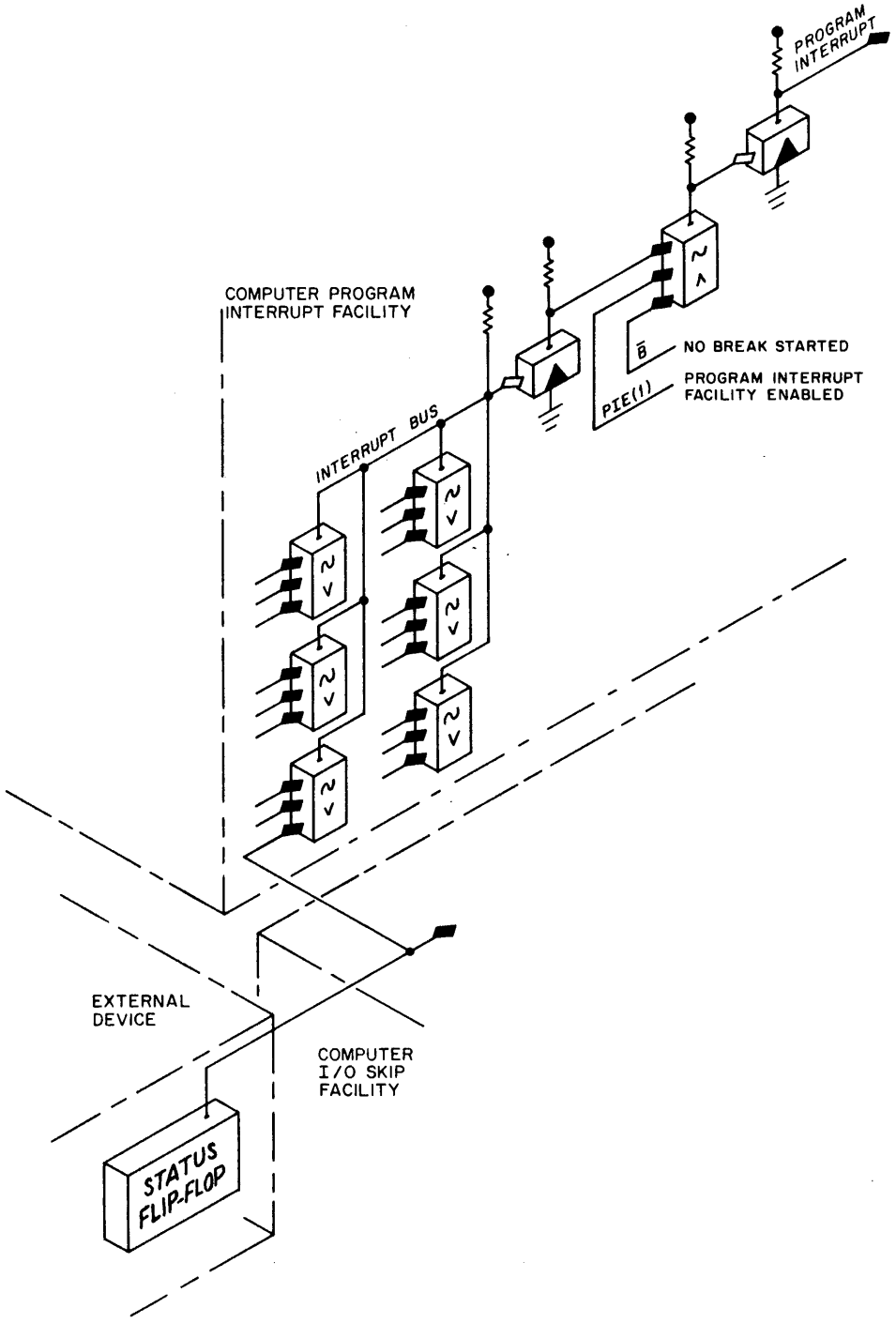


Figure 14 Program Interrupt Facility

If only one device is connected to the PI facility, program control can be transferred directly to a routine that services the device when an interrupt occurs. This operation occurs as follows:

```
Tag     Address   Instruction          Remarks
        1000          .          /MAIN PROGRAM
        1001          .          /MAIN PROGRAM CONTINUES
        1002          .          /INTERRUPT REQUEST OCCURS
                    INTERRUPT OCCURS
        0000                     /LINK, EXTEND AND TRAP FLIP-FLOP STATES,
                                 /EXTENDED PROGRAM COUNT,
                                 /AND PROGRAM COUNT (PC=1003)
                                 /ARE STORED IN 0000
        0001      JMP SR         /ENTER SERVICE ROUTINE
SR      2000          .          /SERVICE SUBROUTINE FOR
                      .          /INTERRUPTING DEVICE AND SEQUENCE TO RESTORE
        3001          .          /AC, AND RESTORE L AND EPC IF REQUIRED
        3002      ION            /TURN ON INTERRUPT
        3003      JMP I 0000     /RETURN TO MAIN PROGRAM
        1003          .          /MAIN PROGRAM CONTINUES
        1004          .
                      .
                      .
```

MULTIPLE USE OF IOS AND PI

In common practice, more than one device is connected to the PI facility. Therefore, since several devices can cause an interrupt, the IOS must identify the device requesting service. When an interrupt occurs, a routine is entered to identify the device requesting an interrupt and to branch to an appropriate service routine. The device can be identified by IOT XX01 pulses that sample a device flags and cause the program to branch or not branch according to the status. Figure 15 shows connections for three typical devices. The following programming example illustrates these functions.

```
Tag     Address   Instruction          Remarks
        1000          .          /MAIN PROGRAM
        1001          .          /MAIN PROGRAM COUNTINUES
        1002          .          /INTERRUPT REQUEST OCCURS
                    INTERRUPT OCCURS
        0000                     /STORE LINK,EPC, AND PC
                                 /(PC=1003)
        0001      JMP FLG CK     /ENTER ROUTINE TO DETERMINE WHICH
                                 /DEVICE CAUSED INTERRUPT
FLG CK            IOT 3401       /SKIP IF DEVICE 34 IS REQUESTING
                  SKP            /NO - TEST NEXT DEVICE
                  JMP SR34       /ENTER SERVICE ROUTINE 34
                  IOT 4401       /SKIP IF DEVICE 44 IS REQUESTING
                  SKP            /NO - TEST NEXT DEVICE
                  JMP SR44       /ENTER SERVICE ROUTINE 44
                  IOT 5401       /SKIP IF DEVICE 54 IS REQUESTING
                  SKP            /NO - TEST NEXT DEVICE
                  JMP SR54       /ENTER SERVICE ROUTINE 54
                      .
                      .
                      .
```

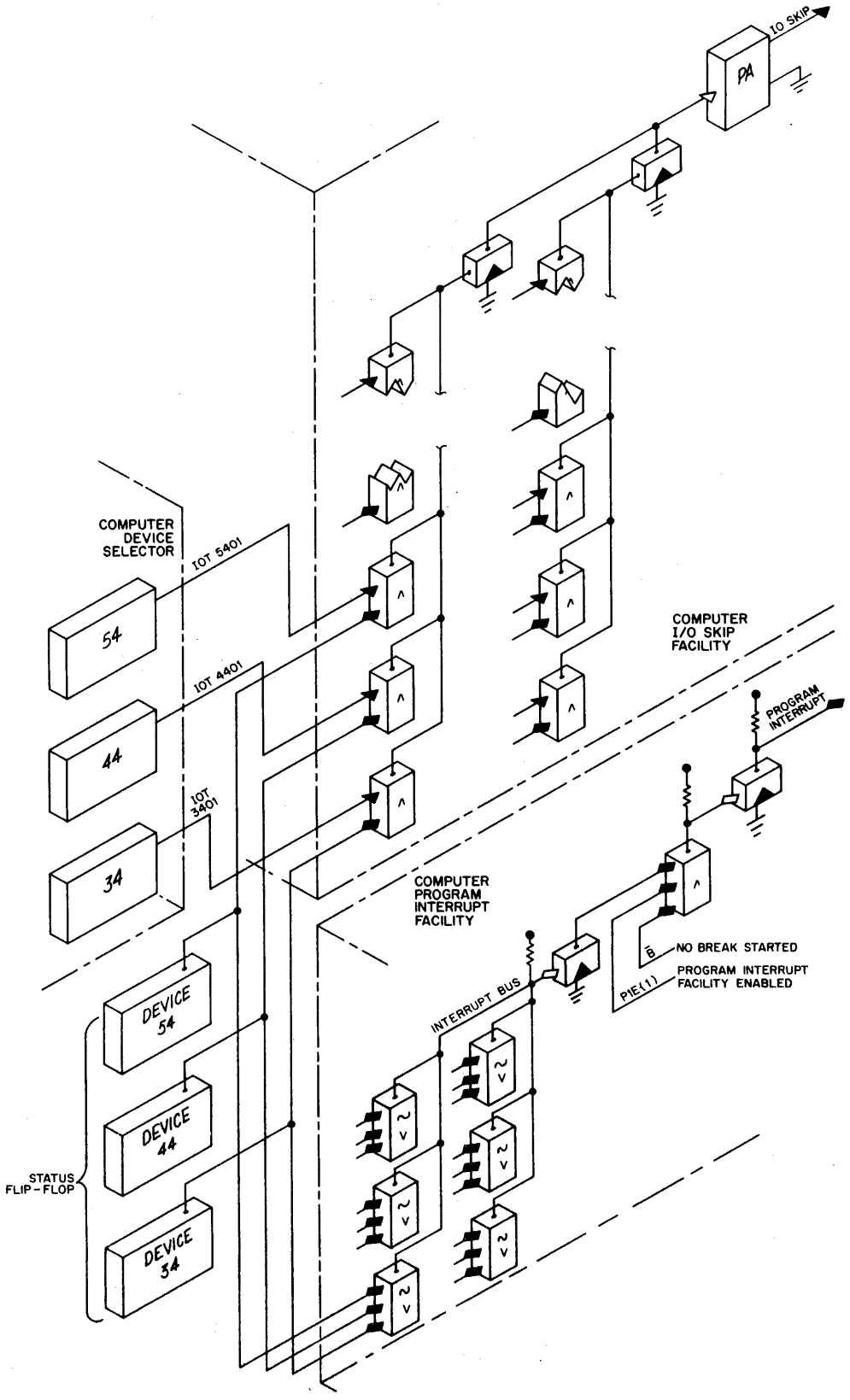


Figure 15 Multiple Use of IOS and PI

Assume that the device that caused the interrupt is an input device (e.g., tape reader). The following example of a device service routine might apply:

```
Tag     Instruction          Remarks
SR      DAC TEMP             /SAVE AC
        IOT XX12             /TRANSFER DATA FROM DEVICE BUFFER TO AC
        DAC I 10             /STORE IN MEMORY LIST
        ISZ COUNT            /CHECK FOR END
        SKP                  /NOT END
        JMP END              /END. JUMP TO ROUTINE TO HANDLE END OF
              .              /LIST CONDITION
              .
              .
                             /RESTORE L AND EPC IF REQUIRED
        LAC TEMP             /RELOAD AC
        ION                  /TURN ON INTERRUPT
        JMP I 0              /RETURN TO PROGRAM
```

If the device that caused the interrupt was essentially an output device (receiving data from computer), the IOT - then - DAC I 10 sequence might be replaced by a LAC I 10 - then - IOT sequence.

EXAMPLE OF PROGRAMMED DATA INPUT AND OUTPUT

The following example, explaining the function and connections of the Teletype unit and Type 649B Teletype control, summarizes interfacing a device with programmed input and output data transfers, using both program interrupt and I/O skip facilities. Figure 16 shows the sequence of operations for a transfer into the computer from the keyboard, and Figure 17 shows the sequence for printing information transferred out of the computer.

Assume that a program is in progress and the keyboard of the Teletype is manually operated to send information into the computer. When the key is struck, the control generates the 8-bit character and shifts it into a keyboard buffer one bit at a time. When the character is complete in the register, the keyboard flag is set to request a program interrupt. If the program interrupt is enabled (meaning the program in operation can be interrupted), when the flag is raised a break occurs at the conclusion of the instruction in progress. During the break cycle the contents of the link, trap mode bit, extended program counter (EPC), and the program counter are stored at core memory address 000000, and the next instruction is taken from address 000001.

This instruction is usually a jump to an interrupt routine which checks the status of flags for all equipment connected into the system. When this routine issues IOT instruction 700301, the 1 status of the keyboard flag is identified and program control jumps to a subroutine that services the keyboard. This subroutine (assuming that the L and EPC need not be restored before returning to the main program) could consist of the following:

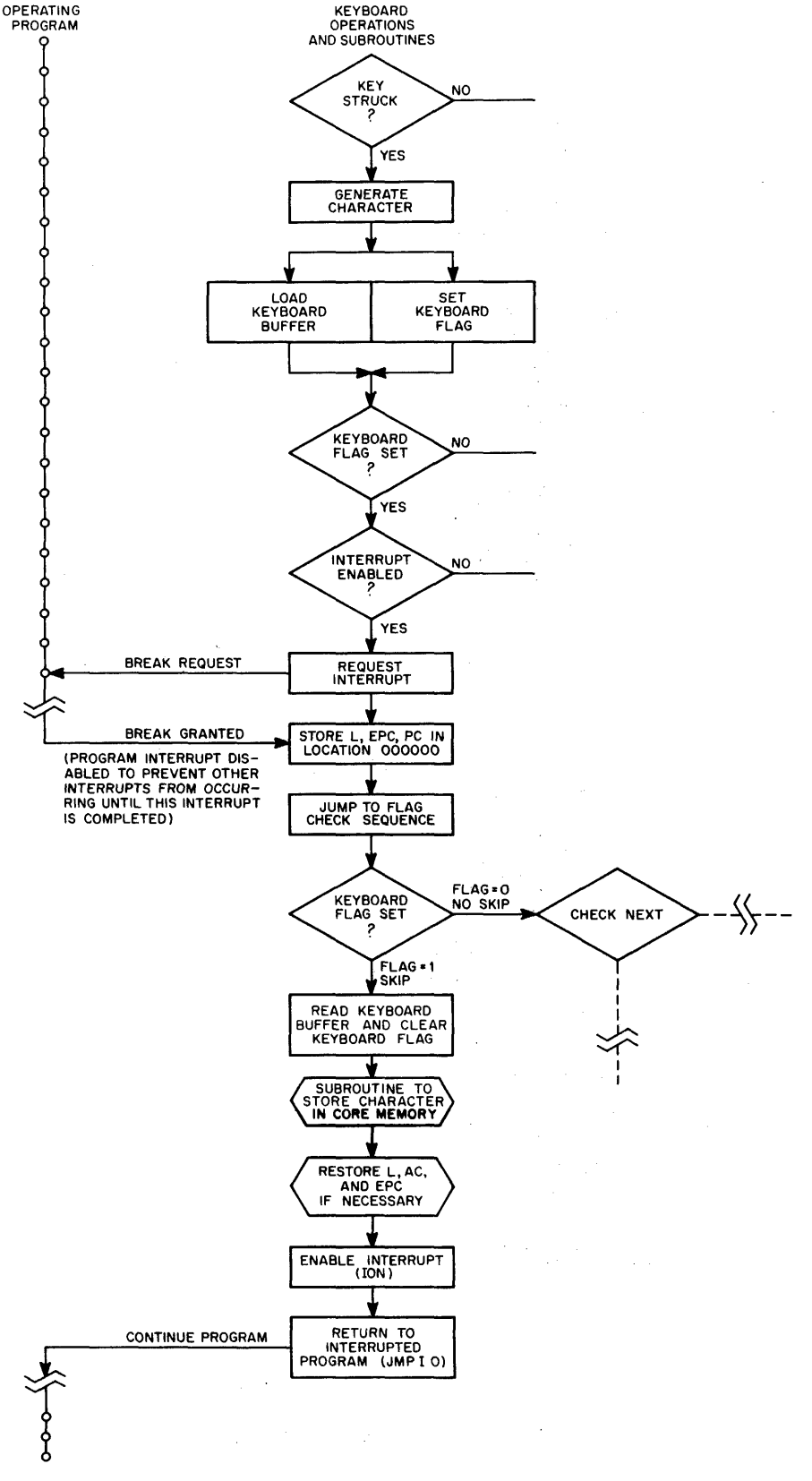


Figure 16 Programmed Data Input Flow Diagram

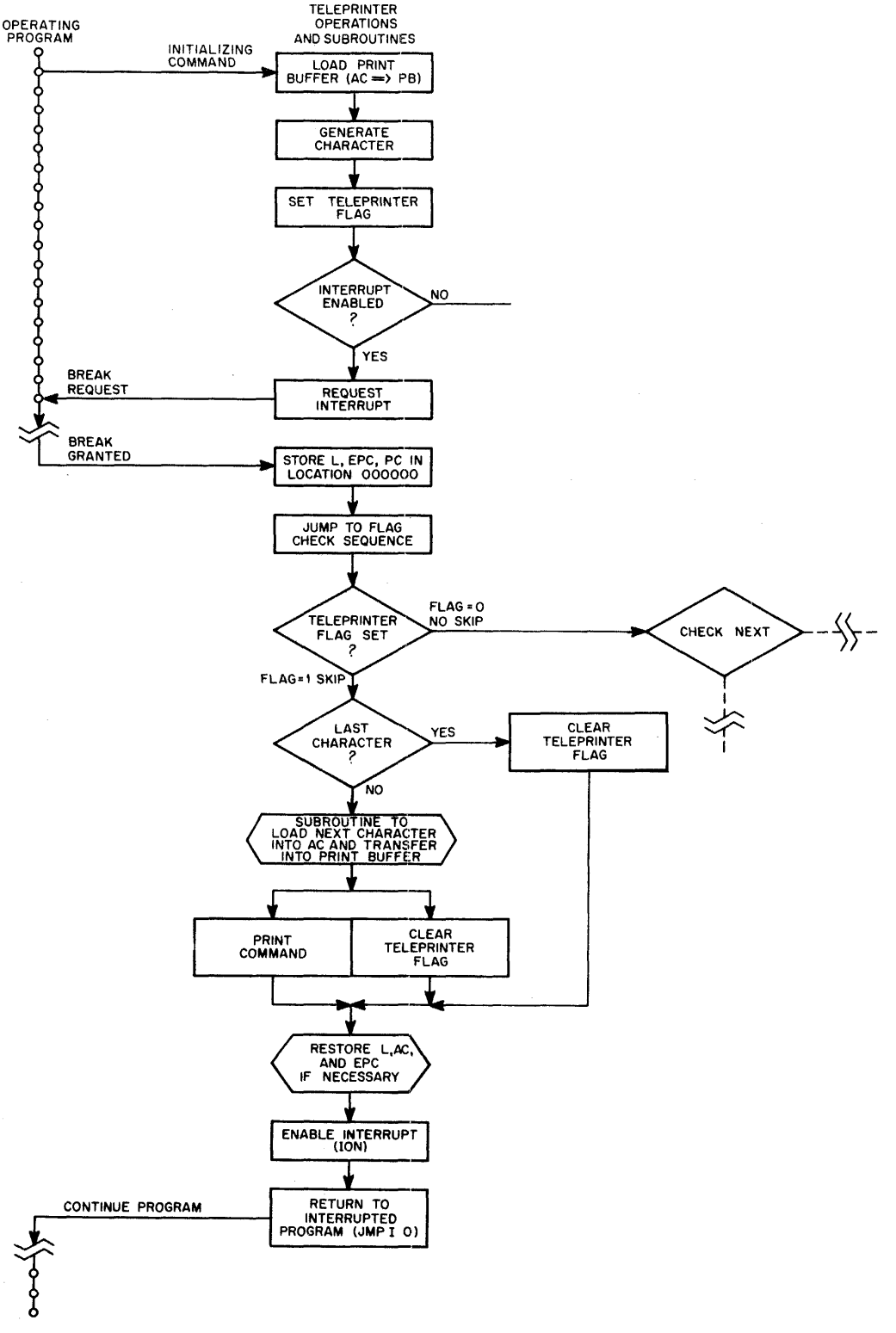


Figure 17 Programmed Data Output Flow Diagram

Octal	Mnemonic	Remarks
700312	KRB	/CLEAR AC, THEN LOAD AC FROM CONTENTS /OF KEYBOARD BUFFER, AND CLEAR KEYBOARD /FLAG
06XXXX	DAC I STORE	/WRITE CHARACTER AT ADDRESS CONTAINED /IN AUTOINDEX REGISTER "STORE"
20XXXX	LAC AC SAVE	/RESTORE AC FROM LOCATION "AC SAVE"
700042	ION	/ENABLE INTERRUPT SYSTEM FOR NEXT CHARACTER
620000	JMP I 0	/RETURN TO MAIN PROGRAM FROM ADDRESS /STORED IN 00000 WHEN BREAK WAS STARTED

Upon completion of this subroutine the main program continues and the keyboard awaits the next manual key operation.

Assume that the main program has accumulated and stored data in core memory, and that the data is to be printed by the Teletype while the main program continues. When the program recognizes the need to print, it initializes a print subroutine (by setting an autoindex register equal to the core memory address -1 for the data, establishing a check for the last character to be printed, initializing a counter to track the number of characters printed, etc.) and then enters the print subroutine to print the first character. The basic print subroutine might be similar to the following:

Octal	Mnemonic	Remarks
22XXXX	LAC I 10	/LOAD CHARACTER INTO AC FROM ADDRESS /SPECIFIED BY AUTOINDEX REGISTER 10
44XXXX	ISZ COUNT	/COUNT CHARACTERS
741000	SKP	/NOT LAST CHARACTER
60XXXX	JMP END	/LAST CHARACTER
700406	TLS	/TRANSFER CHARACTER FROM AC INTO PRINTER /BUFFER, CLEAR PRINTER FLAG, AND INITIATE /PRINTING
	⋮	/RESTORE L AND/OR EPC IF NECESSARY, THEN AC
700042	ION	/ENABLE INTERRUPT SYSTEM FOR NEXT CHARACTER /BREAK
620000	JMP I 0	/RETURN TO MAIN PROGRAM FROM ADDRESS /STORED IN ADDRESS 000000

Exit from this subroutine reestablishes the main program which now continues until interrupted by a program break. Having been initiated by the subroutine, mechanical printing of the first character continues until complete, then raises the print flag. The print flag in the 1 state indicates that the teleprinter has printed the last character and is ready to receive another character, and requests a program interrupt. If the interrupt system is enabled, at the end of the current instruction the break state is entered to store the contents of the L, EPC, and PC in address 000000. The next instruction is then taken from address 000001, and program control is transferred to the interrupt routine. The program interrupt routine, as described

previously for the keyboard, senses the status of flags for all devices connected to the interrupt facility until it determines the device requesting service. When the TSF instruction is given (IOT 700401) to skip on the ready status of the printer flag, the print subroutine is again entered to load and print the next character. At exit from the subroutine the main program is reentered from the point of the program break. If the main program is an arithmetic routine that uses the link or a routine using extended memory, the AC, L, and EPC must be restored by the device service routine prior to issuing the ION instruction. Restoration of the L is accomplished by an instruction sequence such as:

Octal	Mnemonic	Remarks
200000	LAC 0	/LOAD WORD CONTAINING L
740010	RAL	/ROTATE TO RESTORE L

Restoration of the EPC is described in the PDP-7 Users Handbook, F-75, under the description of the Type 148 Memory Extension Control. The AC should always be restored by the service routine.

CHAPTER 3

DATA BREAK TRANSFERS

The data break facility allows one I/O device to transfer information directly with the PDP-7 core memory on a cycle-stealing basis. Up to four devices can connect to the data break facility through the optional Type 173 Data Interrupt Multiplexer.

Data break information transfers occur directly between the computer MB and a data register of the device, and therefore do not affect the arithmetic or program control elements of the PDP-7. Transfer rates of up to 571,000 words per second, or over 10 million bits per second, can be realized through this independent data handling channel.

Figure 18 shows information flow to effect a data break transfer with an I/O device. Figure 19 indicates timing requirements for input and output control and data signals, and the availability of register data signals.

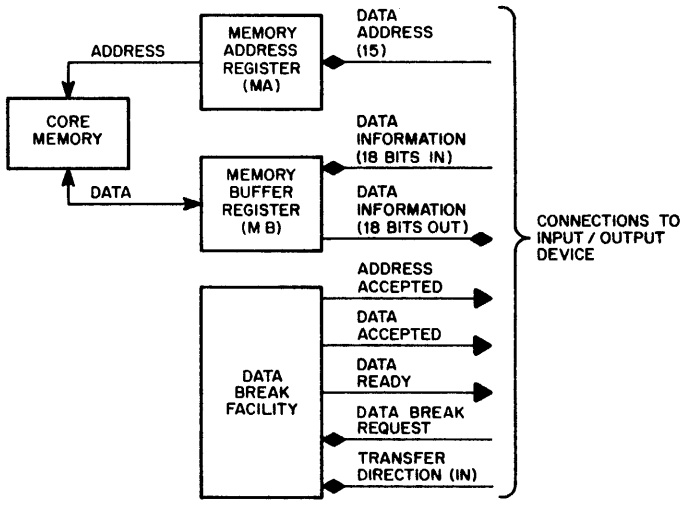


Figure 18 Data Break Transfer Interface Block Diagram

External devices requesting storage or retrieval access to core memory supply the following signals to the computer:

DATA BREAK REQUEST	−3v for assertion
TRANSFER DIRECTION	−3v for into PDP-7, ground for out
DATA ADDRESS (15 bits)	−3v for 1, ground for 0
DATA INFORMATION (18 bits)	−3v for 1, ground for 0

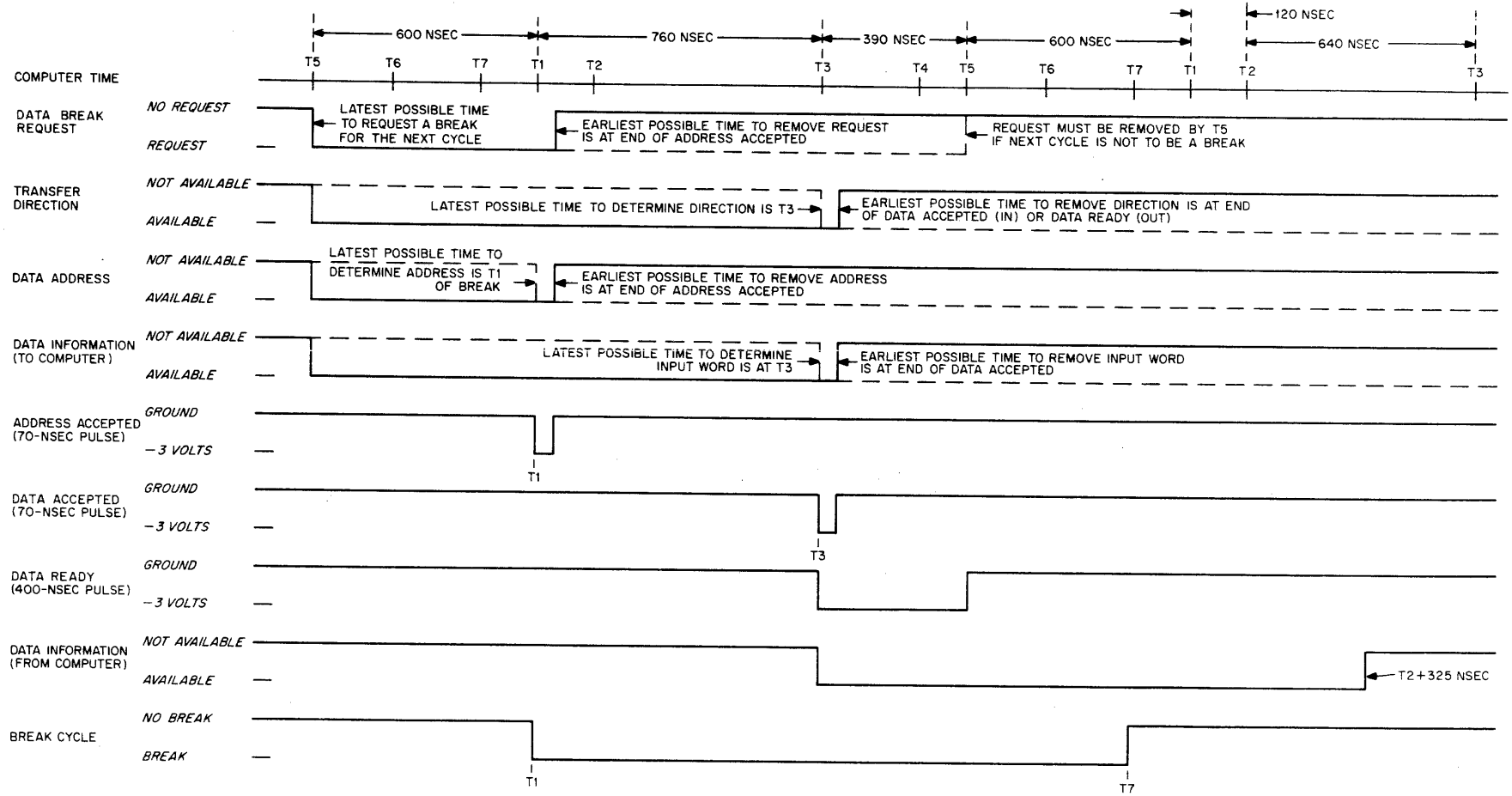


Figure 19 Data Break Transfer Timing Diagram

The computer provides the following signals to the device using the data break facility:

ADDRESS ACCEPTED	Standard DEC 70-nsec negative pulse when device-supplied address is strobed into MA.
DATA ACCEPTED	Standard DEC 70-nsec negative pulse when device-supplied information is strobed into MB.
DATA READY	Standard DEC 400-nsec negative pulse when information is available in MB for strobing by external device. The external device can use this pulse to strobe the MB information into its register either directly or (when gate set-up time is required) after a delay of up to 1 μsec.
DATA INFORMATION (18 bits)	−3v for 1, ground for 0

DATA BREAK FACILITY

The data break facility controls entry into the break state to execute a data break, and produces the pulses that strobe address and data into the computer and indicate data is ready to be strobed out of the computer. Figure 20 shows the interface circuits of the data break facility.

Data break requests are synchronized with the computer timing cycle and the execution of instructions by a DATA SYNC flip-flop. The T5-DLY pulse (T5 delayed 50 nsec) sets this flip-flop if the DATA BREAK REQUEST (or DATA RQ) signal level is at −3v (making a request), or clears it if the request is not made (signal level is at ground). When set, the DATA SYNC flip-flop causes generation of a BK RQ (or BREAK REQUEST) signal level that establishes the break state for the next cycle if the current cycle completes an instruction. Therefore, to initiate a data break the DATA BREAK REQUEST signal must be present (negative) at the time the T5-DLY pulse occurs during the cycle immediately preceding the break. Similarly, when the break is granted the DATA BREAK REQUEST signal must be removed (ground or open) by the time the T5-DLY pulse occurs or the next cycle will also be a break state.

Note that a break state (but not a data break) can also be caused by a program interrupt (PROG SYNC (1) signal) or by the real-time clock (CLK SYNC (1) signal).

The 1 status of the DATA SYNC flip-flop combines with the break condition of the major state generator to produce a DATA • B signal level that enables generation of the ADDRESS ACCEPTED (or ADDR ACC), DATA ACCEPTED (or DATA ACC), and DATA READY (or DATA RDY) pulses.

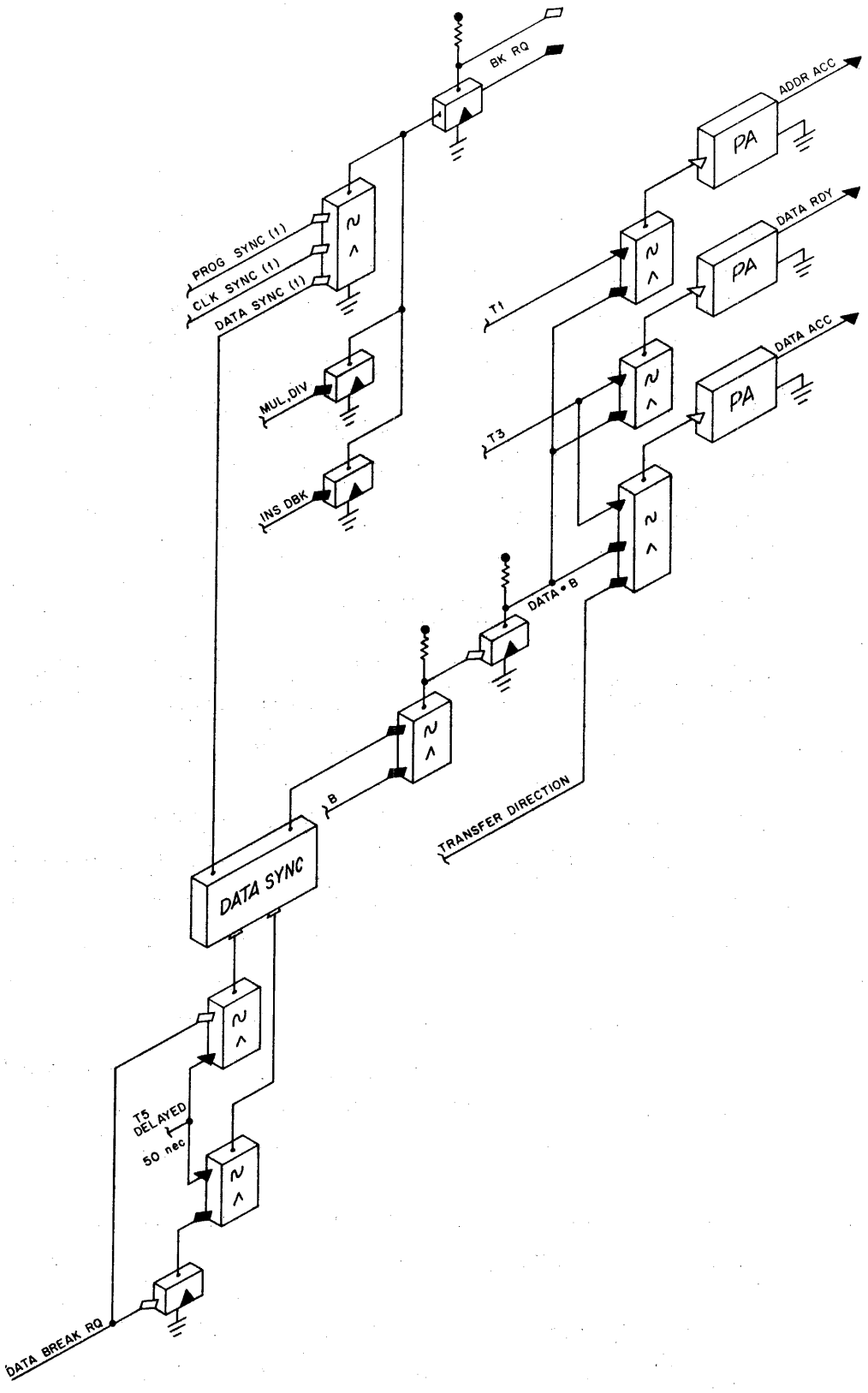


Figure 20 Data Break Facility Interface of Computer

The 70-nsec negative ADDRESS ACCEPTED pulse occurs at T1 time of all data break cycles to strobe the 15 device-supplied DATA ADDRESS signals into the computer MA and EMA (extended MA) registers. This pulse, available at the interface, can be used by the device to remove the DATA BREAK REQUEST signal or to clear or change the data register in preparation for the next cycle.

The 70-nsec negative DATA ACCEPTED pulse occurs at T3 time of the data break cycle if the device-supplied TRANSFER DIRECTION signal level is at −3v to specify a data direction into the computer. This pulse strobes the 18 device-supplied DATA INFORMATION signals into the MB and is available at the interface for use by the device to clear and/or change the data buffer register for the next cycle. The direction of a data break transfer is always stated with respect to the computer. The TRANSFER DIRECTION signal should be −3v to specify a transfer into the PDP-7, or should be ground to specify a transfer out of the PDP-7. This signal should be present at the time the data break request is made; however, it need not be present until T3 of the break cycle.

The 400-nsec negative DATA READY pulse occurs at T3 time of all data break cycles. This pulse is not used in the computer but is produced for the device to use directly, or delayed to allow for gate setup time, to strobe the 18 computer DATA INFORMATION signals into its data buffer register.

DATA ADDRESS

Fifteen DATA ADDRESS (or DA) signals are recieved from the external device to specify the core memory address to be used for the data break transfer. These signals are −3v to signify a binary 1. They should be present when the data break request is made, but may be delayed if they are settled prior to T1 time of the break cycle. These signals are received by a 2-input NAND gate at the 1 input of each MA flip-flop and extended MA flip-flop. Since the MA contains 13 bits, the flip-flops are designated MA5 through MA17. The two extension flip-flops are added to the most significant end of the register and are designated EMA3 and EMA4. Each of these flip-flops is loaded with the information on the DATA ADDRESS lines supplied by the device when the ADDRESS ACCEPTED pulse occurs. The data break facility generates the ADDRESS ACCEPTED pulse at T1 time of a break cycle caused by a negative DATA BREAK REQUEST signal. Figure 21 shows this data address interface logic of the computer.

DATA INFORMATION INPUT AND OUTPUT

Input data from an external device is received by the MB during a data break as 18 DATA INFORMATION (or DI) signal levels. The DATA INFORMATION input signals should be present when the data break request is made, but can be delayed if they are settled prior to T3 time of the break cycle. Each −3v signal (binary 1) enables a 2-input NAND gate at the 1 input of an MB flip-flop. The DATA ACCEPTED

pulse strobes all these gates. This pulse is generated in the data break facility at T3 of the break cycle by negative DATA BREAK REQUEST and TRANSFER DIRECTION signals which request an input data break. Figure 22 shows the data information input interface to the MB.

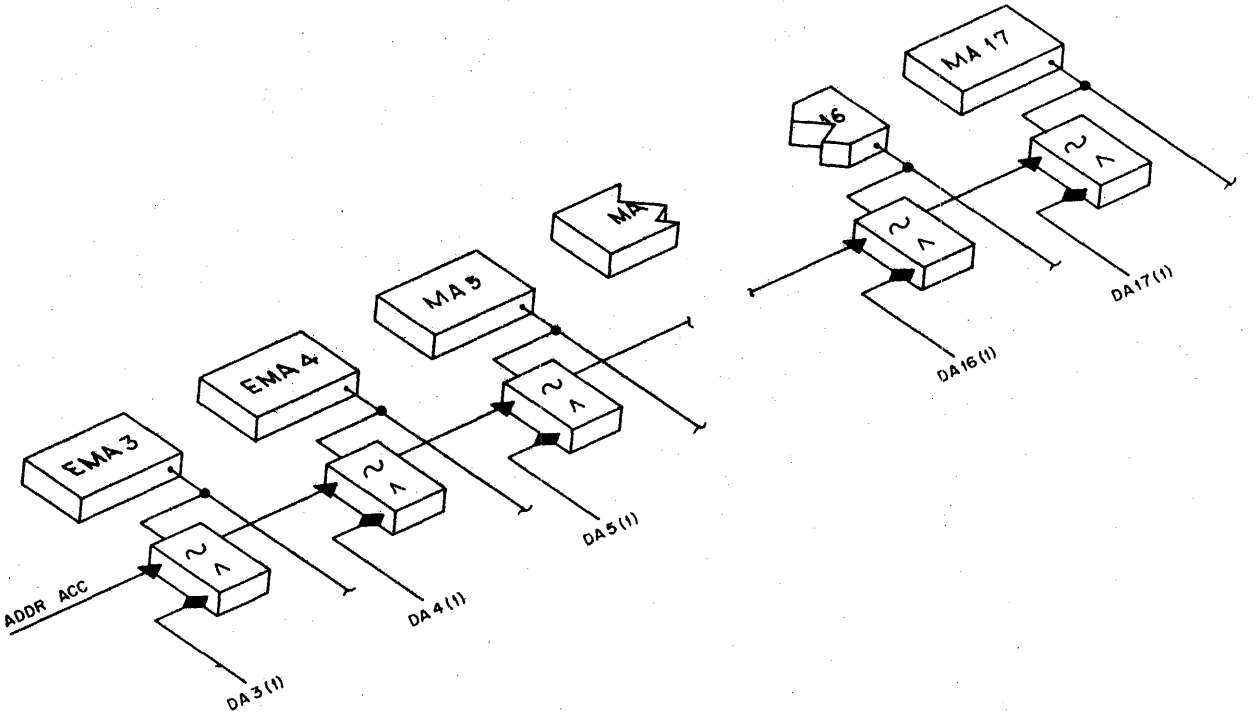


Figure 21 Data Address Input Interface of Computer

Output data from the computer during a data break is supplied to the external device as an 18-bit MB buffered DATA INFORMATION word. The negative binary 1 output of each MB flip-flop is buffered by a non-inverting bus driver and supplied to the interface connection for strobing by the device. The DATA INFORMATION signals are available by T3 time of the break cycle and must be strobed by the DATA READY pulse (or a pulse derived from it) no later than 400 nsec after T2 time of the cycle following the break. Figure 22 also shows this data information interface logic of the computer.

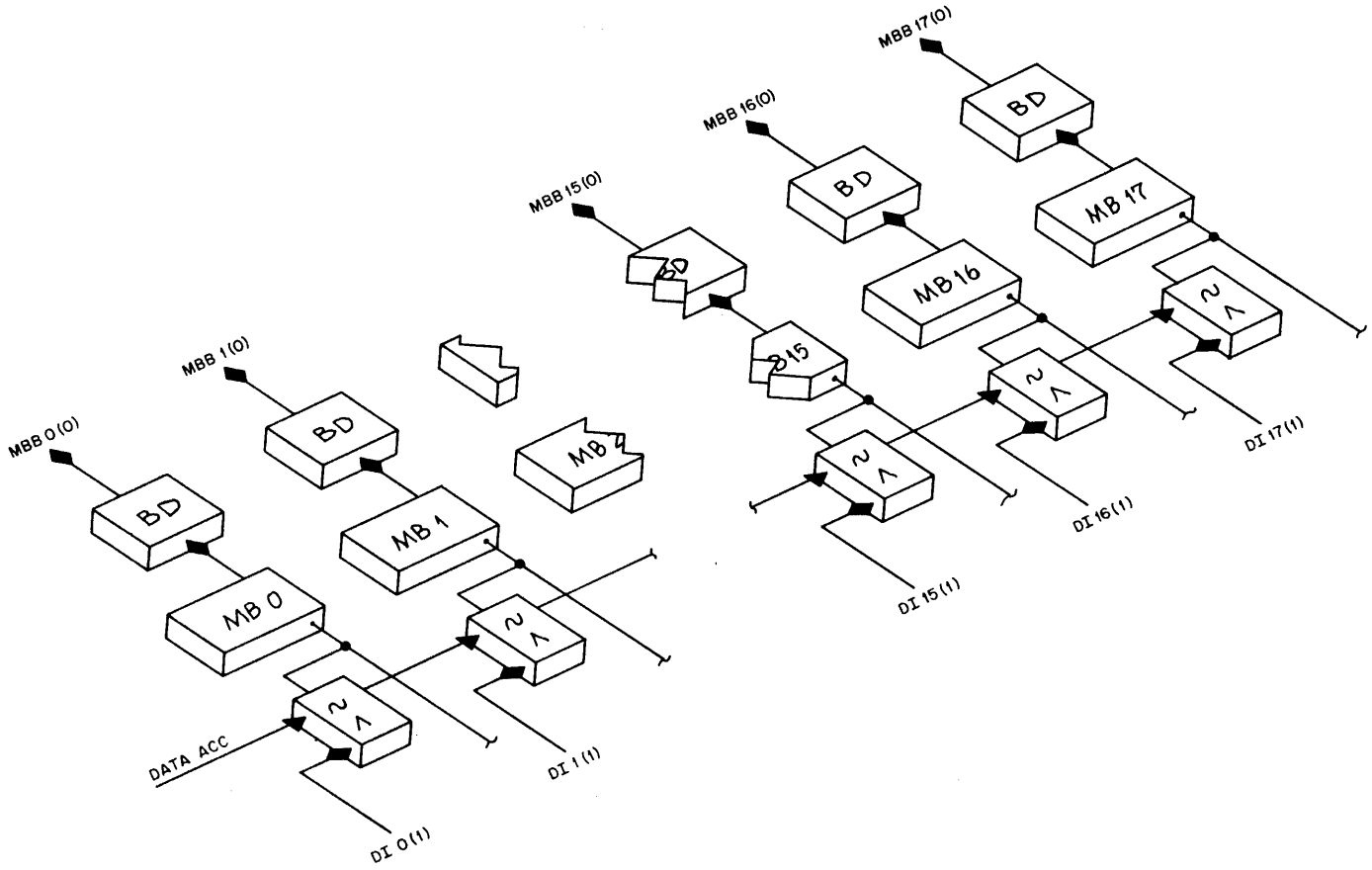


Figure 22 Data Information Input and Output Interface of Computer

CHAPTER 4

DIGITAL LOGIC CIRCUITS

All component circuits in the PDP-7 are standard digital logic circuits as described in the Digital Logic Handbook, C-105. Functional operation of basic circuits, typical applications, and detailed descriptions for the complete line of circuit modules available for construction of interfaces are presented in this catalog. The PDP-7 uses four types of circuits to transmit or receive signals from other equipment--inverters, bus drivers, pulse amplifiers, and diode gates.

INVERTERS

Type B105 Inverter modules are used throughout the computer for gating, inverting, and buffering. The DATA BREAK REQUEST (or DATA RQ) signal is received from external equipment by a B105 in the data break facility. The PROGRAM INTERRUPT REQUEST (or PROGRAM REQ) signal is received from I/O devices by a B124 Inverter module. Internal common collector connections on groups of three inverters facilitate use of this module as a logical NOR gate for negative signal levels.

The Type B201 Flip-Flop modules in both the MA and MB use two series-connected inverters as 2-input NAND gates. Schematically, these inverters are identical to those of the B105 module. In data break transfers, these gates receive the DATA ADDRESS signals in the MA and receive the DATA INFORMATION signals in the MB. In each case the inverter nearest the flip-flop is triggered by an internally generated 70-nsec pulse, and the data signal is received at the inverter with the grounded emitter.

Each inverter is analogous to a switch. If the inverter base is at -3v and the inverter emitter is at ground, the PNP transistor is saturated and a conducting path is established between the emitter and collector. If the base is at ground, the emitter-collector path is open-circuited (i.e., will not allow current to flow) and there is no static load. When the base input is at -3v, the static load is 1 ma. The base can reject 0.5v of noise. Delay through the inverter is approximately 12 nsec for lightly loaded inverters driven by a pulse. Figure 23 shows the inverter circuit schematically.

BUS DRIVERS

Type R650 Bus Driver modules are used by the ID to drive AC output lines in programmed data output transfers. The R650 contains two inverting bus drivers for driving heavy current loads to either ground or negative voltages. In this application, terminals H and S are grounded to insert an integrating capacitor into the circuit to avoid ringing on long lines. The driver operates with typical output rise and fall delays

of 50 nsec, and total transmission time of 800 nsec for output rise and 700 nsec for output fall. If this ground connection is removed, the bus driver operates with typical rise and fall times of 25 nsec, typical total transition times of 60 nsec for output rise and 65 nsec for output fall. The standard DEC level output can drive 20 ma of external load at either ground or −3v. Figure 24 is a schematic of the output circuit of the bus driver.

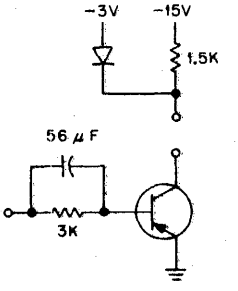


Figure 23 Inverter Circuit

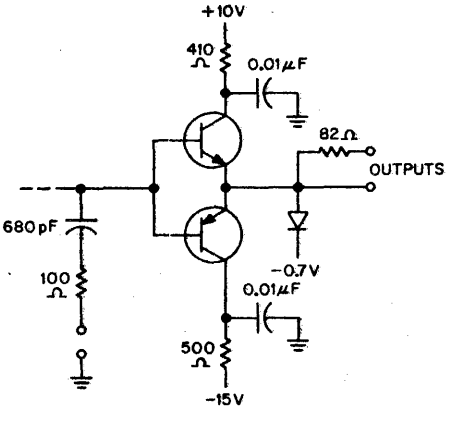


Figure 24 Bus Driver Output Circuit

Type B684 Bus Driver modules are used by the MB to drive the DATA INFORMATION or MBB lines in data break output transfers. The B684 contains two noninverting bus drivers and a −3v supply. Each bus driver provides standard DEC output levels capable of driving ±40 ma. Delay through the driver is approximately 30 nsec. The output circuit is similar to that of the Type R650 shown in Figure 24.

PULSE AMPLIFIERS

Type W640 Pulse Amplifier modules in the DS reproduce or buffer IOT command pulses. The W640 contains three standardizing pulse amplifiers. Delay through the pulse amplifier is approximately 40 nsec. Output pulses can be either 1 μsec (if E and F are connected together) or 400 nsec wide (E and F open). No

connections should be made to terminals E or F (L or M, S or T) other than shorting them together to obtain 1-μsec output pulses. Output is a DEC standard 2.5v, 400-nsec pulse (1 μsec, if E and F are shorted) which occurs every time the input signal meets the input requirement. The output is negative if the positive terminal is grounded. Each output can drive 10 ma of load (equivalent to 10 inverter bases). These amplifiers should not be used without a terminating resistor; typical values are 47 to 150 ohms. A schematic of the output circuit is shown in Figure 25.

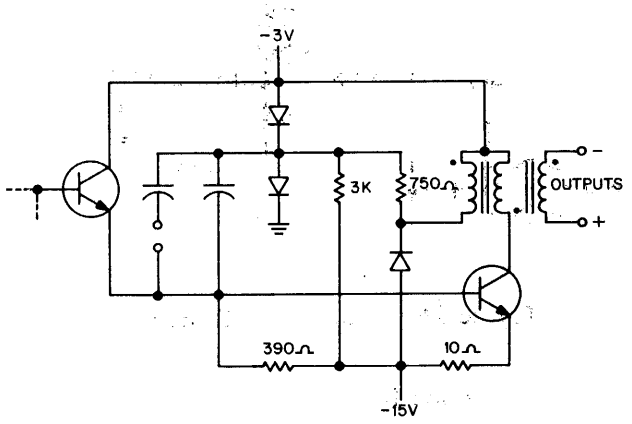


Figure 25 Pulse Amplifier Output Circuit

A Type W607 Pulse Amplifier module in the data break facility provides the ADDR ACC, DATA ACC, and DATA RDY pulses. The W607 contains three standardizing pulse amplifiers. The output is a standard 70-nsec, 2.5v pulse. Delay through the pulse amplifier is approximately 20 nsec. It occurs at the output every time the input signal meets the input requirement. The output is negative if the positive terminal is grounded. Each output can drive 10 ma of load (equivalent to 10 inverter bases). These amplifiers should not be used without a terminating resistor. When driving 1 to 5 ma of load, the line may be terminated by 47 ohms to ground; and when driving 6 to 10 ma of load, 82 ohms to ground. These values are approximate and depend on length of the line. The output circuit is similar to that of the Type W640 shown in Figure 25.

DIODE GATES

Type R141 Diode Gate modules are used in the IC and IOS to receive signals from peripheral devices. The R141 consists of seven 2-input diode AND gates for negative signals whose outputs supply the inputs to a diode NOR gate. Back-to-back diode circuit operations are facilitated by an internal bias resistor connected to the input of each second stage diode. The bias holds the input of the second stage at −3v unless one of the first stage inputs is grounded. The total transition time is 45 nsec for output rise and 70 nsec for output fall. The input receives standard 100-nsec pulses, standard levels of −3v and ground,

or 70 nsec negative pulses. Input load is 1 ma per input pair shared by the grounded inputs. When any pair of inputs is not being used, at least one of the two must be grounded. Figure 26 shows the basic circuit configuration.

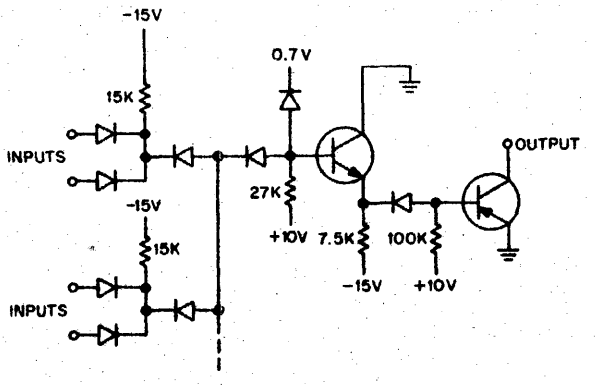


Figure 26 Diode Gate Circuit

A Type B171 Diode Gate module is used in the I/O package to receive SLOW CYCLE REQUEST signals. The B171 is a 12-input diode NOR gate for ground level signals. An additional inverter allows complementary output signals. Typical total transition time is 40 nsec for output fall and 60 nsec for output rise. Static input load is 1.25 ma.

A Type B115 Diode Gate module in the data break facility receives the TRANSFER DIRECTION (DATA IN) signal from the external device. The B115 consists of three 3-input diode NAND gates for negative signals. The TRANSFER DIRECTION signal supplies one input to one of these gates. The remaining two inputs are supplied by a negative level and a negative timing pulse produced within the computer. The 1.25-ma static load is shared by all inputs at ground.

CHAPTER 5

INTERFACE CONNECTIONS

INTERFACE CONNECTIONS AND SIGNAL IDENTIFICATION

All signals interchanged between the PDP-7 processor and the peripheral equipment pass through the interface section of the I/O package in the computer. Interface connections are made either by coaxial cable or by ribbon cables terminated in a Type W021 Signal Cable Connector (described in detail in the Digital Logic Handbook, C-105). The cable connector plugs into the appropriate FLIP CHIP module receptacles in rows H and J of bay 3 (containing the I/O package). Figure 27 shows the relative location and signals assigned to these connectors. Some cable connections, for the Type 177B EAE option for example, are made directly to the processor in bay 2. In general, all interface connections to the processor are made through the I/O package, except for options that are normally installed at the factory when the system is built.

In any system, bays are numbered from left to right as viewed from the front. Rows of modules are lettered from top to bottom within one prewired option. Module receptacles are numbered from left to right as viewed from the wiring side at the front of the machine or from right to left as viewed from the module side at the back of the machine. Terminals of a module receptacle are assigned capital letters from top to bottom, omitting G, I, O, and Q. For example, A03E in the I/O package is in the top module row (A), the third connector from the left (03), and the fifth terminal from the top (E).

All logic signals that pass between the PDP-7 and the I/O equipment are standard DEC levels or standard DEC pulses. Logic signals have mnemonic names that indicate the condition represented by assertion of the signal. Standard levels are either ground potential (0.0 to −0.3v) designated by an open diamond (——◇) or are −3v (−3v to −4.0v) designated by a solid diamond (——◆). Standard pulses in the positive direction are designated by an open triangle (——▷), and negative pulses are designated by a solid triangle (——▶). Pulses originating in R series modules are positive-going pulses which start at −3v, go to ground for 100 nsec, then return to −3v. Pulses originating in B or W series modules are bipolar, are always referenced to ground, are 2.5v in amplitude (2.3 to 3.0v) with a 2v overshoot, and are of 400-nsec duration (or 1 μsec if selected on the W640).

Tables 1 and 2 provide connections, distribution, and logic circuit information for the basic PDP-7 interface signals. Numbers in the "Drawing Number" column of these tables should be prefixed by "BS-D-KA1A-0-" or "BS-D-KA77A-0-" to form the complete number of engineering drawing that shows

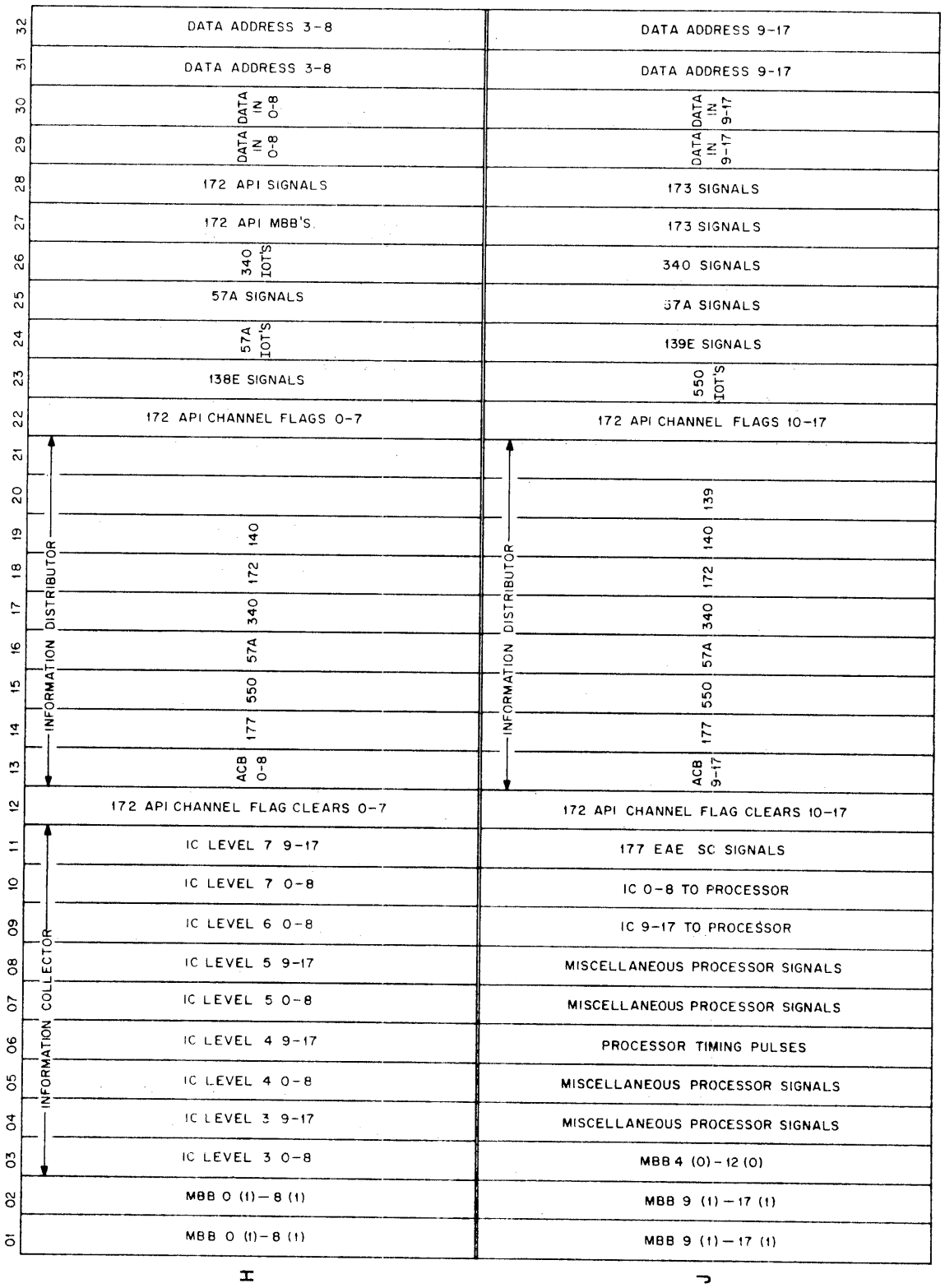


Figure 27 Interface Cable Connector Locations and Assignments

signal destination or signal origin in the I/O package or processor. Table 3 lists the prewired interface terminals and connectors. This prewiring simplifies installation of standard PDP-7 options. Because of the large number of options available, there is redundancy in the interface-connector wiring. This redundancy has been planned so that two options not likely to be included in the same system use a common connector. Some wiring changes and/or ground jumper disconnections are required when connecting any device which the interface connectors are not prewired to receive. Note that alternate terminals of the Type W021 Signal Cable Connectors carry ground lines for cable shields. These grounds on terminals C, F, J, L, N, R, and U are not listed in Table 3.

LOADING AND DRIVING CONSIDERATIONS

All interface circuits within the PDP-7 consist of series R and W FLIP CHIP modules. When interconnecting these circuits with those in the peripheral equipment, it is important to keep the load on each circuit within its driving ability. Driving and loading capabilities of most DEC modules used in the PDP-7 and in standard DEC optional equipment are specified in detail in the Digital FLIP CHIP Modules Catalog, C-105.

All inputs to series R modules consist of either diode gate or diode-capacitor-diode (DCD) gate circuits. All inputs draw current in the same direction. Each diode gate input at ground level draws 1 ma. The output of a diode gate with an internal clamped load resistor can drive an 18-ma external load. A flip-flop consists of two cross-connected diode gates. The direct set and clear terminals draw 1 ma. The output capability is 20 ma, less 2 ma for the load resistor permanently connected in the flip-flop, and 1 ma required to condition the opposite side of the flip-flop. The flip-flop can, therefore, drive a 17-ma external load.

The DCD gate circuits on flip-flops and pulse amplifiers draw 2 ma at the level inputs, 3 ma at the pulse inputs when the level is conditioned, and 1 ma when the level input is disabled. When two DCD gates are driving both sides of the same flip-flop, the load on both pulse inputs totals only 4 ma. When the level inputs are tied together as in a complement configuration, the total input load is only 3 ma.

Capacitive loading adversely affects the performance of series R modules; therefore, where long lines are being driven, extra clamped loads should be added to sufficiently discharge the cable capacitance. As a general rule, an extra 2 ma of clamped-load current should be added for every foot of wire beyond 1-1/2 ft. An exception to this rule is the R650 Bus Driver module. This module is designed to drive coaxial cable of 100-ohm characteristic impedance through a series driving resistor. If coaxial cable is not used, the direct output may be used when the lines are short. If reflections occur on the line, the resistive output of the bus driver may be used to correct the problem. Shunt termination on the far end of the transmission line is not recommended.

TABLE 1 INPUT SIGNALS

Signal	Symbol	Signal Destination in I/O Package KA71A					Signal Destination in Processor KA77A			
		Interface Connector	Module Terminal	Module Type	Logic Element	Drawing Number	Module Terminal	Module Type	Logic Element	Drawing Number
RB00(1)			E01F	R141	IC	4				
RB01(1)			E02F	R141	IC	4				
RB02(1)			E03F	R141	IC	4				
RB03(1)			E04F	R141	IC	4				
RB04(1)			E05F	R141	IC	4				
RB05(1)			E06F	R141	IC	4				
RB06(1)			E07F	R141	IC	4				
RB07(1)			E08F	R141	IC	4				
RB08(1)			E09F	R141	IC	4				
RB09(1)			F01F	R141	IC	4				
RB10(1)			F02F	R141	IC	4				
RB11(1)			F03F	R141	IC	4				
RB12(1)			F04F	R141	IC	4				
RB13(1)			F05F	R141	IC	4				
RB14(1)			F06F	R141	IC	4				
RB15(1)			F07F	R141	IC	4				
RB16(1)			F08F	R141	IC	4				

TABLE 1 INPUT SIGNALS (continued)

Signal	Symbol	Signal Destination in I/O Package KA71A					Signal Destination in Processor KA77A			
		Interface Connector	Module Terminal	Module Type	Logic Element	Drawing Number	Module Terminal	Module Type	Logic Element	Drawing Number
RB17(1)	—◆		F09F	R141	IC	4				
MQ00(1)	—◆	H03D	E01L	R141	IC	4				
MQ01(1)	—◆	H03E	E02L	R141	IC	4				
MQ02(1)	—◆	H03H	E03L	R141	IC	4				
MQ03(1)	—◆	H03K	E04L	R141	IC	4				
MQ04(1)	—◆	H03M	E05L	R141	IC	4				
MQ05(1)	—◆	H03P	E06L	R141	IC	4				
MQ06(1)	—◆	H03S	E07L	R141	IC	4				
MQ07(1)	—◆	H03T	E08L	R141	IC	4				
MQ08(1)	—◆	H03V	E09L	R141	IC	4				
MQ09(1)	—◆	H04D	F01L	R141	IC	4				
MQ10(1)	—◆	H04E	F02L	R141	IC	4				
MQ11(1)	—◆	H04H	F03L	R141	IC	4				
MQ12(1)	—◆	H04K	F04L	R141	IC	4				
MQ13(1)	—◆	H04M	F05L	R141	IC	4				
MQ14(1)	—◆	H04P	F06L	R141	IC	4				

TABLE 1 INPUT SIGNALS (continued)

Signal	Symbol	Signal Destination in I/O Package KA71A					Signal Destination in Processor KA77A			
		Interface Connector	Module Terminal	Module Type	Logic Element	Drawing Number	Module Terminal	Module Type	Logic Element	Drawing Number
MQ15(1)	◆—	H04S	F07L	R141	IC	4				
MQ16(1)	◆—	H04T	F08L	R141	IC	4				
MQ17(1)	◆—	H04V	F09L	R141	IC	4				
DTI00(1)	◆—	1H05D	E01N	R141	IC	4				
DTI01(1)	◆—	1H05E	E02N	R141	IC	4				
DTI02(1)	◆—	1H05H	E03N	R141	IC	4				
DTI03(1)	◆—	1H05K	E04N	R141	IC	4				
DTI04(1)	◆—	1H05M	E05N	R141	IC	4				
DTI05(1)	◆—	1H05P	E06N	R141	IC	4				
DTI06(1)	◆—	1H05S	E07N	R141	IC	4				
DTI07(1)	◆—	1H05T	E08N	R141	IC	4				
DTI08(1)	◆—	1H05V	E09N	R141	IC	4				
DTI09(1)	◆—	1H06D	F01N	R141	IC	4				
DTI10(1)	◆—	1H06E	F02N	R141	IC	4				
DTI11(1)	◆—	1H06H	F03N	R141	IC	4				
DTI12(1)	◆—	1H06K	F04N	R141	IC	4				

TABLE 1 INPUT SIGNALS (continued)

Signal	Symbol	Signal Destination in I/O Package KA71A					Signal Destination in Processor KA77A			
		Interface Connector	Module Terminal	Module Type	Logic Element	Drawing Number	Module Terminal	Module Type	Logic Element	Drawing Number
DTI13(1)	◆—	1H06M	F05N	R141	IC	4				
DTI14(1)	◆—	1H06P	F06N	R141	IC	4				
DTI15(1)	◆—	1H06S	F07N	R141	IC	4				
DTI16(1)	◆—	1H06T	F08N	R141	IC	4				
DTI17(1)	◆—	1H06V	F09N	R141	IC	4				
CA03(1)	◆—	H07K	E04R	R141	IC	4				
CA04(1)	◆—	H07M	E05R	R141	IC	4				
CA05(1)	◆—	H07P	E06R	R141	IC	4				
CA06(1)	◆—	H07S	E07R	R141	IC	4				
CA07(1)	◆—	H07T	E08R	R141	IC	4				
CA08(1)	◆—	H07V	E09R	R141	IC	4				
CA09(1)	◆—	H08D	F01R	R141	IC	4				
CA10(1)	◆—	H08E	F02R	R141	IC	4				
CA11(1)	◆—	H08H	F03R	R141	IC	4				
CA12(1)	◆—	H08K	F04R	R141	IC	4				
CA13(1)	◆—	H08M	F05R	R141	IC	4				

TABLE 1 INPUT SIGNALS (continued)

Signal	Symbol	Signal Destination in I/O Package KA71A					Signal Destination in Processor KA77A			
		Interface Connector	Module Terminal	Module Type	Logic Element	Drawing Number	Module Terminal	Module Type	Logic Element	Drawing Number
CA14(1)	—◆	H08D	F06R	R141	IC	4				
CA15(1)	—◆	H08S	F07R	R141	IC	4				
CA16(1)	—◆	H08T	F08R	R141	IC	4				
CA17(1)	—◆	H08V	F09R	R141	IC	4				
DATA FLG	—◆	H09D	E01T	R141	IC	4				
BLK FLG	—◆	H09E	E02T	R141	IC	4				
ERR FLG	—◆	H09F	E03T	R141	IC	4				
OFF END	—◆	H09K	E04T	R141	IC	4				
MISS IND	—◆	H09M	E05T	R141	IC	4				
REV STATUS	—◆	H09P	E06T	R141	IC	4				
GO	—◆	H09S	E07T	R141	IC	4				
MRK TRK ERR	—◆	H09T	E08T	R141	IC	4				
UNABLE	—◆	H09V	E09T	R141	IC	4				
DR LATE	—◆	H10D	E01V	R141	IC	4				
PARITY ERR	—◆	H10E	E02V	R141	IC	4				
READ COMP ERR	—◆	H10H	E03V	R141	IC	4				

TABLE 1 INPUT SIGNALS (continued)

Signal	Symbol	Signal Destination in I/O Package KA71A					Signal Destination in Processor KA77A			
		Interface Connector	Module Terminal	Module Type	Logic Element	Drawing Number	Module Terminal	Module Type	Logic Element	Drawing Number
EOF	◆—	H10K	E04V	R141	IC	4				
WRITE LOCK	◆—	H10M	E05V	R141	IC	4				
LOAD POINT	◆—	H10P	E06V	R141	IC	4				
END POINT	◆—	H10S	E07V	R141	IC	4				
TRD/WR LR	◆—	H10T	E08V	R141	IC	4				
A/B FR	◆—	H10V	E09V	R141	IC	4				
TTI00(1)	◆—		F02T	R141	IC	4				
TTI01(1)	◆—		F03T	R141	IC	4				
TTI02(1)	◆—		F04T	R141	IC	4				
TTI03(1)	◆—		F05T	R141	IC	4				
TTI04(1)	◆—		F06T	R141	IC	4				
TTI05(1)	◆—		F07T	R141	IC	4				
TTI06(1)	◆—		F08T	R141	IC	4				
TTI07(1)	◆—		F09T	R141	IC	4				
REWIND	◆—	H11D	F01V	R141	IC	4				
MISS CHAR	◆—	H11E	F02V	R141	IC	4				

TABLE 1 INPUT SIGNALS (continued)

Signal	Symbol	Signal Destination in I/O Package KA71A					Signal Destination in Processor KA77A			
		Interface Connector	Module Terminal	Module Type	Logic Element	Drawing Number	Module Terminal	Module Type	Logic Element	Drawing Number
57A JOB DONE	◆—	H11H	F03V	R141	IC	4				
(F04V)	◆—	H11K	F04V	R141	IC	4				
(F05V)	◆—	H11M	F05V	R141	IC	4				
(F06V)	◆—	H11P	F06V	R141	IC	4				
(F07V)	◆—	H11S	F07V	R141	IC	4				
(F08V)	◆—	H11T	F08V	R141	IC	4				
(F09V)	◆—	H11V	F09V	R141	IC	4				
PIE(1)B	◆—		E01J	R141	IC					
RDR FLG(1)	◆—		E02J	R141	IC					
PUN FLG(1)	◆—		E03J	R141	IC					
KBD FLG(1)	◆—		E04J	R141	IC					
F PRINTER FLG(1)	◆—		E05J	R141	IC					
DPY FLG(1)	◆—		E06J	R141	IC					
CLK FLG(1)	◆—		E07J	R141	IC					
CLK EN(1)	◆—		E08J	R141	IC					
57A JOB DONE(1)	◆—		E09J	R141	IC					

TABLE 1 INPUT SIGNALS (continued)

Signal	Symbol	Signal Destination in I/O Package KA71A					Signal Destination in Processor KA77A			
		Interface Connector	Module Terminal	Module Type	Logic Element	Drawing Number	Module Terminal	Module Type	Logic Element	Drawing Number
SC12(1)			F04J	R141	IC					
SC13(1)			F05J	R141	IC					
SC14(1)			F06J	R141	IC					
SC15(1)			F07J	R141	IC					
SC16(1)			F08J	R141	IC					
SC17(1)			F09J	R141	IC					
EIC00	⟶	E13D	E01D	R141	IC	4				
EIC01	⟶	E13E	E02D	R141	IC	4				
EIC02	⟶	E13H	E03D	R141	IC	4				
EIC03	⟶	E13K	E04D	R141	IC	4				
EIC04	⟶	E13M	E05D	R141	IC	4				
EIC05	⟶	E13P	E06D	R141	IC	4				
EIC06	⟶	E13S	E07D	R141	IC	4				
EIC07	⟶	E13T	E08D	R141	IC	4				
EIC08	⟶	E13V	E09D	R141	IC	4				
EIC09	⟶	F13D	F01D	R141	IC	4				

TABLE 1 INPUT SIGNALS (continued)

Signal	Symbol	Signal Destination in I/O Package KA71A					Signal Destination in Processor KA77A			
		Interface Connector	Module Terminal	Module Type	Logic Element	Drawing Number	Module Terminal	Module Type	Logic Element	Drawing Number
EIC10	→	F13E	F02D	R141	IC	4				
EIC11	→	F13H	F03D	R141	IC	4				
EIC12	→	F13K	F04D	R141	IC	4				
EIC13	→	F13M	F05D	R141	IC	4				
EIC14	→	F13P	F06D	R141	IC	4				
EIC15	→	F13S	F07D	R141	IC	4				
EIC16	→	F13T	F08D	R141	IC	4				
EIC17	→	F13V	F09D	R141	IC	4				
DA03	◆→	H32K				11	C18M	B201	MA	15
DA04	◆→	H32M				11	C19M	B201	MA	15
DA05	◆→	H32P				11	C20M	B201	MA	15
DA06	◆→	H32S				11	C21M	B201	MA	15
DA07	◆→	H32T				11	C22M	B201	MA	15
DA08	◆→	H32V				11	C23M	B201	MA	15
DA09	◆→	J32D				11	C24M	B201	MA	15
DA10	◆→	J32E				11	C25M	B201	MA	15

TABLE 1 INPUT SIGNALS (continued)

Signal	Symbol	Signal Destination in I/O Package KA71A					Signal Destination in Processor KA77A			
		Interface Connector	Module Terminal	Module Type	Logic Element	Drawing Number	Module Terminal	Module Type	Logic Element	Drawing Number
DA11	◆—	J32H				11	C26M	B201	MA	15
DA12	◆—	J32K				11	C27M	B201	MA	15
DA13	◆—	J32M				11	C28M	B201	MA	15
DA14	◆—	J32P				11	C29M	B201	MA	15
DA15	◆—	J32S				11	C30M	B201	MA	15
DA16	◆—	J32T				11	C31M	B201	MA	15
DA17	◆—	J32V				11	C32M	B201	MA	15
DI00(1)	◆—	H30D				11	E02M	B201	MB	16
DI01(1)	◆—	H30E				11	E03M	B201	MB	16
DI02(1)	◆—	H30H				11	E04M	B201	MB	16
DI03(1)	◆—	H30K				11	E05M	B201	MB	16
DI04(1)	◆—	H30M				11	E06M	B201	MB	16
DI05(1)	◆—	H30P				11	E07M	B201	MB	16
DI06(1)	◆—	H30S				11	E08M	B201	MB	16
DI07(1)	◆—	H30T				11	E09M	B201	MB	16
DI08(1)	◆—	H30V				11	E10M	B201	MB	16

TABLE 1 INPUT SIGNALS (continued)

Signal	Symbol	Signal Destination in I/O Package KA71A					Signal Destination in Processor KA77A			
		Interface Connector	Module Terminal	Module Type	Logic Element	Drawing Number	Module Terminal	Module Type	Logic Element	Drawing Number
DI09(1)	◆→	J30D				11	E11M	B201	MB	16
DI10(1)	◆→	J30E				11	E12M	B201	MB	16
DI11(1)	◆→	J30H				11	E13M	B201	MB	16
DI12(1)	◆→	J30K				11	E14M	B201	MB	16
DI13(1)	◆→	J30M				11	E15M	B201	MB	16
DI14(1)	◆→	J30P				11	E16M	B201	MB	16
DI15(1)	◆→	J30S				11	E17M	B201	MB	16
DI16(1)	◆→	J30T				11	E18M	B201	MB	16
DI17(1)	◆→	J30V				11	E19M	B201	MB	16
IC00(1)	→	J10D				4	HJ2JL	B210	AC	17
IC01(1)	→	J10E				4	HJ3JL	B210	AC	17
IC02(1)	→	J10H				4	HJ4JL	B210	AC	17
IC03(1)	→	J10K				4	HJ5JL	B210	AC	17
IC04(1)	→	J10M				4	HJ6JL	B210	AC	17
IC05(1)	→	J10P				4	HJ7JL	B210	AC	17
IC06(1)	→	J10S				4	HJ8JL	B210	AC	17

TABLE 1 INPUT SIGNALS (continued)

Signal	Symbol	Signal Destination in I/O Package KA71A					Signal Destination in Processor KA77A			
		Interface Connector	Module Terminal	Module Type	Logic Element	Drawing Number	Module Terminal	Module Type	Logic Element	Drawing Number
IC07(1)	→	J10T				4	HJ9JL	B210	AC	17
IC08(1)	→	J10V				4	HJ10JL	B210	AC	17
IC09(1)	→	J11D				4	HJ11JL	B210	AC	17
IC10(1)	→	J11E				4	HJ12JL	B210	AC	17
IC11(1)	→	J11H				4	HJ13JL	B210	AC	17
IC12(1)	→	J11K				4	HJ14JL	B210	AC	17
IC13(1)	→	J11M				4	HJ15JL	B210	AC	17
IC14(1)	→	J11P				4	HJ16JL	B210	AC	17
IC15(1)	→	J11S				4	HJ17JL	B210	AC	17
IC16(1)	→	J11T				4	HJ18JL	B210	AC	17
IC17(1)	→	J11V				4	HJ19JL	B210	AC	17
IOT 0102(B)	→		E01E	R141	IC	4				
IOT 0304(B)	→		E01H	R141	IC	4				
MQ1 → AC	→		E01K	R141	IC	4				
IOT 7502	→	J23E	E01M	R141	IC	4				
IOT 7404	→		E01P	R141	IC	4				

TABLE 1 INPUT SIGNALS (continued)

Signal	Symbol	Signal Destination in I/O Package KA71A					Signal Destination in Processor KA77A			
		Interface Connector	Module Terminal	Module Type	Logic Element	Drawing Number	Module Terminal	Module Type	Logic Element	Drawing Number
IOT 7602	→		E01S	R141	IC	4				
IOT 7304	→		E01U	R141	IC	4				

TABLE 2 OUTPUT SIGNALS

Signal	Symbol	Signal Origin in I/O Package KA71A					Signal Origin in Processor KA77A			
		Interface Connector	Module Terminal	Module Type	Logic Element	Drawing Number	Module Terminal	Module Type	Logic Element	Drawing Number
ACB00(1)	—◇	H14D-H21D		W021	ID	11	M03J	R650	AC Bus Drivers	18
ACB01(1)	—◇	H14E-H21E		W021	ID	11	M03T	R650	AC Bus Drivers	18
ACB02(1)	—◇	H14H-H21H		W021	ID	11	M04J	R650	AC Bus Drivers	18
ACB03(1)	—◇	H14K-H21K		W021	ID	11	M04T	R650	AC Bus Drivers	18
ACB04(1)	—◇	H14M-H21M		W021	ID	11	M05J	R650	AC Bus Drivers	18
ACB05(1)	—◇	H14P-H21P		W021	ID	11	M05T	R650	AC Bus Drivers	18
ACB06(1)	—◇	H14S-H21S		W021	ID	11	M06J	R650	AC Bus Drivers	18
ACB07(1)	—◇	H14T-H21T		W021	ID	11	M06T	R650	AC Bus Drivers	18
ACB08(1)	—◇	H14V-H21V		W021	ID	11	M07J	R650	AC Bus Drivers	18
ACB09(1)	—◇	J14D-J21D		W021	ID	11	M07T	R650	AC Bus Drivers	18
ACB10(1)	—◇	J14E-J21E		W021	ID	11	M08J	R650	AC Bus Drivers	18
ACB11(1)	—◇	J14H-J21H		W021	ID	11	M08T	R650	AC Bus Drivers	18
ACB12(1)	—◇	J14K-J21K		W021	ID	11	M09J	R650	AC Bus Drivers	18
ACB13(1)	—◇	J14M-J21M		W021	ID	11	M09T	R650	AC Bus Drivers	18
ACB14(1)	—◇	J14P-J21P		W021	ID	11	M10J	R650	AC Bus Drivers	18
ACB15(1)	—◇	J14S-J21S		W021	ID	11	M10T	R650	AC Bus Drivers	18

TABLE 2 OUTPUT SIGNALS (continued)

Signal	Symbol	Signal Origin in I/O Package KA71A					Signal Origin in Processor KA77A			
		Interface Connector	Module Terminal	Module Type	Logic Element	Drawing Number	Module Terminal	Module Type	Logic Element	Drawing Number
ACB16(1)	—◇	J14T-J13T		W021	ID	11	M11J	R650	AC Bus Drivers	18
ACB17(1)	—◇	J14V-J13V		W021	ID	11	M11T	R650	AC Bus Drivers	18
IOT0002	—▷		D25F	R603	DS	5				
IOT0004	—▷		D25M	R603	DS	5				
IOT0102	—▷		D21T	R603	DS	5				
IOT0104	—▷		D21F	R603	DS	5				
IOT0202	—▷		D22M	R603	DS	5				
IOT0204	—▷		D22T	R603	DS	5				
IOT0302	—▷		D23F	R603	DS	5				
IOT0304	—▷		D23M	R603	DS	5				
IOT0402	—▷		D23T	R603	DS	5				
IOT0404	—▷		D24F	R603	DS	5				
IOT0502	—▷		C23F	R603	DS	5				
IOT0504	—▷		C23M	R603	DS	5				
IOT0602	—▷		C23T	R603	DS	5				
IOT0604	—▷		C24F	R603	DS	5				

TABLE 2 OUTPUT SIGNALS (continued)

Signal	Symbol	Signal Origin in I/O Package KA71A					Signal Origin in Processor KA77A			
		Interface Connector	Module Terminal	Module Type	Logic Element	Drawing Number	Module Terminal	Module Type	Logic Element	Drawing Number
IOT0702	⟶▷		C24M	R603	DS	5				
IOT0704	⟶▷		C24T	R603	DS	5				
IOT0002(B)	⟶	J07B	D29U	W640	DS	5				
IOT0004(B)	⟶	H28M	D29N	W640	DS	5				
IOT0102(B)	⟶		F14H	W640	DS	5				
IOT0302(B)	⟶		F14N	W640	DS	5				
IOT0304(B)	⟶		F14U	W640	DS	5				
IOT0502(B)	⟶		E32H	W640	DS	6				
IOT0504(B)	⟶	H26K	E32N	W640	DS	6				
IOT0602(B)	⟶	H26D	E32U	W640	DS	6				
IOT0604(B)	⟶	H26E	F32H	W640	DS	6				
IOT0702(B)	⟶		F32V	W640	DS	6				
IOT0704(B)	⟶	H26H	F32U	W640	DS	6				
IOT1001	⟶		D32H	W640	DS	6				
IOT1002	⟶		D32N	W640	DS	6				
IOT1004	⟶		D32U	W640	DS	6				

TABLE 2 OUTPUT SIGNALS (continued)

Signal	Symbol	Signal Origin in I/O Package KA71A					Signal Origin in Processor KA77A			
		Interface Connector	Module Terminal	Module Type	Logic Element	Drawing Number	Module Terminal	Module Type	Logic Element	Drawing Number
IOT1101	→	J24D	F30H	W640	DS	6				
IOT1102	→	J24E	F30N	W640	DS	6				
IOT1104	→		E30H	W640	DS	6				
IOT1201	→	J24H	F30U	W640	DS	6				
IOT1202	→		E31N	W640	DS	6				
IOT1204	→		E31U	W640	DS	6				
IOT1301	→		F31H	W640	DS	6				
IOT1302	→	H23E	F31N	W640	DS	6				
IOT1304	→	H23K	F31U	W640	DS	6				
IOT2101	→		E27H	W640	DS	6				
IOT2102	→		E27N	W640	DS	6				
IOT2104	→		E27U	W640	DS	6				
IOT7002	→	H24D	F27H	W640	DS	6				
IOT7004	→	H24E	F27N	W640	DS	6				
IOT7102	→	H24H	F27U	W640	DS	6				
IOT7104	→	H24K	E28H	W640	DS	6				

TABLE 2 OUTPUT SIGNALS (continued)

Signal	Symbol	Signal Origin in I/O Package KA71A					Signal Origin in Processor KA77A			
		Interface Connector	Module Terminal	Module Type	Logic Element	Drawing Number	Module Terminal	Module Type	Logic Element	Drawing Number
IOT7202	→	H24M	E28N	W640	DS	6				
IOT7204	→	H24P	E28U	W640	DS	6				
IOT7301	→		F28H	W640	DS	6				
IOT7302	→	H24S	F28N	W640	DS	6				
IOT7304	→		F28U	W640	DS	6				
IOT7401	→	H24T	E29H	W640	DS	6				
IOT7402	→	H24V	E29N	W640	DS	6				
IOT7404	→	H25D	E29U	W640	DS	6				
IOT7501	→	J23D	F29H	W640	DS	6				
IOT7502	→	J23E	F29N	W640	DS	6				
IOT7504	→	J23H	F29U	W640	DS	6				
IOT7601	→		E30H	W640	DS	6				
IOT7602	→		E30N	W640	DS	6				
IOT7604	→	J23K	E30U	W640	DS	6				
MBB04(0)	◆→	J03D				11	D07D	B684	MB Bus Drivers	18
MBB05(0)	◆→	J03E				11	D07N	B684	MB Bus Drivers	18

TABLE 2 OUTPUT SIGNALS (continued)

Signal	Symbol	Signal Origin in I/O Package KA71A					Signal Origin in Processor KA77A			
		Interface Connector	Module Terminal	Module Type	Logic Element	Drawing Number	Module Terminal	Module Type	Logic Element	Drawing Number
MBB06(B)		J03H				11	D09D	B684	MB Bus Drivers	18
MBB07(0)		J03K				11	D09N	B684	MB Bus Drivers	18
MBB08(0)		J03M				11	D11D	B684	MB Bus Drivers	18
MBB09(0)		J03P				11	D11N	B684	MB Bus Drivers	18
MBB10(0)		J03S				11	D13D	B684	MB Bus Drivers	18
MBB11(0)		J03T				11	D13N	B684	MB Bus Drivers	18
MBB12(0)		J03V				11	D15D	B684	MB Bus Drivers	18
MBB00(1)		H02D		W21	ID	11	D22D	B684	MB Bus Drivers	18
MBB01(1)		H02E		W21	ID	11	D22N	B684	MB Bus Drivers	18
MBB02(1)		H02H		W21	ID	11	D23D	B684	MB Bus Drivers	18
MBB03(1)		H02K		W21	ID	11	D23N	B684	MB Bus Drivers	18
MBB04(1)		H02M		W21	ID	11	D24D	B684	MB Bus Drivers	18
MBB05(1)		H02P		W21	ID	11	D24N	B684	MB Bus Drivers	18
MBB06(1)		H02S		W21	ID	11	D25D	B684	MB Bus Drivers	18
MBB07(1)		H02T		W21	ID	11	D25N	B684	MB Bus Drivers	18
MBB08(1)		H02V		W21	ID	11	D26D	B684	MB Bus Drivers	18

TABLE 2 OUTPUT SIGNALS (continued)

Signal	Symbol	Signal Origin in I/O Package KA71A					Signal Origin in Processor KA77A			
		Interface Connector	Module Terminal	Module Type	Logic Element	Drawing Number	Module Terminal	Module Type	Logic Element	Drawing Number
MBB09(1)	◆—	J02D		W21	ID	11	D26N	B684	MB Bus Drivers	18
MBB10(1)	◆—	J02E		W21	ID	11	D27D	B684	MB Bus Drivers	18
MBB11(1)	◆—	J02H		W21	ID	11	D27N	B684	MB Bus Drivers	18
MBB12(1)	◆—	J02K		W21	ID	11	D28D	B684	MB Bus Drivers	18
MBB13(1)	◆—	J02M		W21	ID	11	D28N	B684	MB Bus Drivers	18
MBB14(1)	◆—	J02P		W21	ID	11	D29D	B684	MB Bus Drivers	18
MBB15(1)	◆—	J02S		W21	ID	11	D29N	B684	MB Bus Drivers	18
MBB16(1)	◆—	J02T		W21	ID	11	D30D	B684	MB Bus Drivers	18
MBB17(1)	◆—	J02V		W21	ID	11	D30N	B684	MB Bus Drivers	18

TABLE 3 PREWIRED INTERFACE CONNECTIONS

Signal	Terminal	Signal	Terminal
	57A Automatic Magnetic Tape Control		
ACB 00(1)	H16D	ACB 09(1)	J16D
ACB 01(1)	H16E	ACB 10(1)	J16E
ACB 02(1)	H16H	ACB 11(1)	J16H
ACB 03(1)	H16K	ACB 12(1)	J16K
ACB 04(1)	H16M	ACB 13(1)	J16M
ACB 05(1)	H16P	ACB 14(1)	J16P
ACB 06(1)	H16S	ACB 15(1)	J16S
ACB 07(1)	H16T	ACB 16(1)	J16T
ACB 08(1)	H16V	ACB 17(1)	J16V
IOT 7002	H24D	IOT 7404	H25D
IOT 7004	H24E	PWR CLR NEG	H25E
IOT 7102	H24H	BGN (B)	H25H
IOT 7104	H24K	MBB 12(1)	H25K
IOT 7202	H24M	MBB 12(0)	H25M
IOT 7204	H24P		H25P
IOT 7302	H24S		H25S
IOT 7401	H24T		H25T
IOT 7402	H24V		H25V
ERF-ERF ENB	J25D		H07D
WC0-WC0 ENG	J25E		H07E
TCR	J25H		H07H
T READY	J25K	CA 03(1)	H07K
DATA ACC	J25M	CA 04(1)	H07M
ADDRESS ACC	J25P	CA 05(1)	H07P
DATA IN	J25S	CA 06(1)	H07S
DATA RQ	J25T	CA 07(1)	H07T
	J25V	CA 08(1)	H07V

TABLE 3 PREWIRED INTERFACE CONNECTIONS (continued)

Signal	Terminal	Signal	Terminal
	57A Automatic Magnetic Tape Control (continued)		
CA 09(1)	H08D	DR LATE	H10D
CA 10(1)	H08E	PARITY ERR	H10E
CA 11(1)	H08H	READ COMP ERR	H10H
CA 12(1)	H08K	EOF	H10K
CA 13(1)	H08M	WRITE LOCK	H10M
CA 14(1)	H08P	LOAD POINT	H10P
CA 15(1)	H08S	END POINT	H10S
CA 16(1)	H08T	TRD/WR LR	H10T
CA 17(1)	H08V	A/B FR	H10V
REWIND	H11D		
MISS CHAR	H11E		
57A JOB DONE	H11H		
(F04V)	H11K		
(F05V)	H11M		
(F06V)	H11P		
(F07V)	H11S		
(F08V)	H11T		
(F09V)	H11V		
	138 Analog-to-Digital Converter		
	H10D		H11D
	H10E		H11E
	H10H		H11H
	H10K	(F04V)	H11K
	H10M	(F05V)	H11M
	H10P	(F06V)	H11P
	H10S	(F07V)	H11S
	H10T	(F08V)	H11T
	H10V	(F09V)	H11V

TABLE 3 PREWIRED INTERFACE CONNECTIONS (continued)

Signal	Terminal	Signal	Terminal
	138 Analog-to-Digital Converter (continued)		
	H23D		
	H23E		
	H23H		
(F04V)	H23K		
(F05V)	H23M		
(F06V)	H23P		
(F07V)	H11S		
(F08V)	H11T		
(F09V)	H11V		
	139 Multiplexer		
ACB 09(1)	J20D	IOT 1101	J24D
ACB 10(1)	J20E	IOT 1102	J24E
ACB 11(1)	J20H	IOT 1201	J24H
ACB 12(1)	J20K	CA 12(1)	J24K
ACB 13(1)	J20M	CA 13(1)	J24M
ACB 14(1)	J20P	CA 14(1)	J24P
ACB 15(1)	J20S	CA 15(1)	J24S
ACB 16(1)	J20T	CA 16(1)	J24T
ACB 17(1)	J20V	CA 17(1)	J24V
	140 Relay Buffer		
ACB 00(1)	H19D	ACB 09(1)	J19D
ACB 01(1)	H19E	ACB 10(1)	J19E
ACB 02(1)	H19H	ACB 11(1)	J19H
ACB 03(1)	H19K	ACB 12(1)	J19K
ACB 04(1)	H19M	ACB 13(1)	J19M
ACB 05(1)	H19P	ACB 14(1)	J19P
ACB 06(1)	H19S	ACB 15(1)	J19S
ACB 07(1)	H19T	ACB 16(1)	J19T
ACB 08(1)	H19V	ACB 17(1)	J19V

TABLE 3 PREWIRED INTERFACE CONNECTIONS (continued)

Signal	Terminal	Signal	Terminal
	172 Automatic Priority Interrupt		
Clear Flag 0-7	H12D	Clear Flag 8-17	J12D
Clear Flag 0-7	H12E	Clear Flag 8-17	J12E
Clear Flag 0-7	H12H	Clear Flag 8-17	J12H
Clear Flag 0-7	H12K	Clear Flag 8-17	J12K
Clear Flag 0-7	H12M	Clear Flag 8-17	J12M
Clear Flag 0-7	H12P	Clear Flag 8-17	J12P
Clear Flag 0-7	H12S	Clear Flag 8-17	J12S
Clear Flag 0-7	H12T	Clear Flag 8-17	J12T
Clear Flag 0-7	H12V	Clear Flag 8-17	J12V
ACB 00(1)	H18D	ACB 09(1)	J18D
ACB 01(1)	H18E	ACB 10(1)	J18E
ACB 02(1)	H18H	ACB 11(1)	J18H
ACB 03(1)	H18K	ACB 12(1)	J18K
ACB 04(1)	H18M	ACB 13(1)	J18M
ACB 05(1)	H18P	ACB 14(1)	J18P
ACB 06(1)	H18S	ACB 15(1)	J18S
ACB 07(1)	H18T	ACB 16(1)	J18T
ACB 08(1)	H18V	ACB 17(1)	J18V
Channel Flag 0-7	H22D	Channel Flag 8-17	J22D
Channel Flag 0-7	H22E	Channel Flag 8-17	J22E
Channel Flag 0-7	H22H	Channel Flag 8-17	J22H
Channel Flag 0-7	H22K	Channel Flag 8-17	J22K
Channel Flag 0-7	H22M	Channel Flag 8-17	J22M
Channel Flag 0-7	H22P	Channel Flag 8-17	J22P
Channel Flag 0-7	H22S	Channel Flag 8-17	J22S
Channel Flag 0-7	H22T	Channel Flag 8-17	J22T
Channel Flag 0-7	H22V	Channel Flag 8-17	J22V

TABLE 3 PREWIRED INTERFACE CONNECTIONS (continued)

Signal	Terminal	Signal	Terminal
	172 Automatic Priority Interrupt (continued)		
MBB 06(1)	H27D	IOP1	H28D
MBB 07(0)	H27E	IOP2	H28E
MBB 08(1)	H27H	IOP4	H28H
MBB 09(1)	H27K	CLK FLG (1)	H28K
MBB 10(0)	H27M	IOT 0004 (B)	H28M
MBB 10(1)	H27P	PWR CLR NEG	H28P
MBB 11(0)	H27S	BGN (B)	H28S
MBB 11(1)	H27T	MB 12(0)	H28T
	H27V	IOT 00 EN	H28V
	173 Data Interrupt Multiplexer Control		
T5	J28D		
T6	J28E		
DATA RQ	J28H		
DATA IN	J28K		
DATA ACC	J28M		
ADDR ACC	J28P		
DATA RDY	J28S		
DATA SLO RQ	J28T		
	J28V		
	177 Extended Arithmetic Element		
MQ 00(1)	H03D	MQ 09(1)	H04D
MQ 01(1)	H03E	MQ 10(1)	H04E
MQ 02(1)	H03H	MQ 11(1)	H04H
MQ 03(1)	H03K	MQ 12(1)	H04K
MQ 04(1)	H03M	MQ 13(1)	H04M
MQ 05(1)	H03P	MQ 14(1)	H04P
MQ 06(1)	H03S	MQ 15(1)	H04S
MQ 07(1)	H03T	MQ 16(1)	H04T
MQ 08(1)	H03V	MQ 17(1)	H04V

TABLE 3 PREWIRED INTERFACE CONNECTIONS (continued)

Signal	Terminal	Signal	Terminal
	177 Extended Arithmetic Element (continued)		
ACB 00(1)	H14D	ACB 09(1)	J14D
ACB 01(1)	H14E	ACB 10(1)	J14E
ACB 02(1)	H14H	ACB 11(1)	J14H
ACB 03 (1)	H14K	ACB 12(1)	J14K
ACB 04(1)	H14M	ACB 13(1)	J14M
ACB 05(1)	H14P	ACB 14(1)	J14P
ACB 06(1)	H14S	ACB 15(1)	J14S
ACB 07(1)	H14T	ACB 16(1)	J14T
ACB 08(1)	H14V	ACB 17(1)	J14V
SC1-AC	J11D		
MQ1-AC	J11E		
	J11H		
SC 12(1)	J11K		
SC 13(1)	J11M		
SC 14(1)	J11P		
SC 15(1)	J11S		
SC 16(1)	J11T		
SC 17(1)	J11V		
	340 Precision Incremental Display		
	H10D		H11D
	H10E		H11E
	H10H		H11H
	H10K	(F04V)	H11K
	H10M	(F05V)	H11M
	H10P	(F06V)	H11P
	H10S	(F07V)	H11S
	H10T	(F08V)	H11T
	H10V	(F09V)	H11V

TABLE 3 PREWIRED INTERFACE CONNECTIONS (continued)

Signal	Terminal	Signal	Terminal
		340 Precision Incremental Display (continued)	
ACB 00(1)	H17D	ACB 09(1)	J17D
ACB 01(1)	H17E	ACB 10(1)	J17E
ACB 02(1)	H17H	ACB 11(1)	J17H
ACB 03(1)	H17K	ACB 12(1)	J17K
ACB 04(1)	H17M	ACB 13(1)	J17M
ACB 05(1)	H17P	ACB 14(1)	J17P
ACB 06(1)	H17S	ACB 15(1)	J17S
ACB 07(1)	H17T	ACB 16(1)	J17T
ACB 08(1)	H17V	ACB 17(1)	J17V
IOT 0602 (B)	H26D	STOP FIG	J26D
IOT 0604 (B)	H26E	340 LP FLG	J26E
IOT 0704 (B)	H26H	DATA RQ	J26H
IOT 0504 (B)	H26K	DATA IN	J26K
	H26M	ADDR ACC	J26M
	H26P	DATA ACC	J26P
	H26S	BGN	J26S
	H26T	V EDGE FLG	J26T
	H26V	H EDGE FLG	J26V
		550 DECtape Control	
DTI 00(1)	H05D	DTI 09(1)	H06D
DTI 01(1)	H05E	DTI 10(1)	H06E
DTI 02(1)	H05H	DTI 11(1)	H06H
DTI 03(1)	H05K	DTI 12(1)	H06K
DTI 04(1)	H05M	DTI 13(1)	H06M
DTI 05(1)	H05P	DTI 14(1)	H06P
DTI 06(1)	H05S	DTI 15(1)	H06S
DTI 07(1)	H05T	DTI 16(1)	H06T
DTI 08(1)	H05V	DTI 17(1)	H06V

TABLE 3 PREWIRED INTERFACE CONNECTIONS (continued)

Signal	Terminal	Signal	Terminal
	550 DECtape Control (continued)		
ACB 00(1)	H15D	ACB 09(1)	J15D
ACB 01(1)	H15E	ACB 10(1)	J15E
ACB 02(1)	H15H	ACB 11(1)	J15H
ACB 03(1)	H15K	ACB 12(1)	J15K
ACB 04(1)	H15M	ACB 13(1)	J15M
ACB 05(1)	H15P	ACB 14(1)	J15P
ADB 06(1)	H15S	ACB 15(1)	J15S
ACB 07(1)	H15T	ACB 16(1)	J15T
ACB 08(1)	H15V	ACB 17(1)	J15V
DATA FLG	H09D	IOT 7501	J23D
BLK FLG	H09E	IOT 7502	H23E
ERR FLG	H09H	IOT 7504	H23H
OFF END	H09K	IOT 7604	H23K
MISS IND	H09M	RUN (1) B	H23M
REV STATUS	H09P	MBB 12(1)	H23P
GO	H09S	550 IOT 7501	H23S
MK TRK ERR	H09T	550 IOT 7541	H23T
UNABLE	H09V	PWR CLR NEG	H23V
	Unspecified Data Break Device		
MBB 00(1)	H02D	MBB 09(1)	J02D
MBB 01(1)	H02E	MBB 10(1)	J02E
MBB 02(1)	H02H	MBB 11(1)	J02H
MBB 03(1)	H02K	MBB 12(1)	J02K
MBB 04(1)	H02M	MBB 13(1)	J02M
MBB 05(1)	H02P	MBB 14(1)	J02P
MBB 06(1)	H02S	MBB 15(1)	J02S
MBB 07(1)	H02T	MBB 16(1)	J02T
MBB 08(1)	H02V	MBB 17(1)	J02V

TABLE 3 PREWIRED INTERFACE CONNECTIONS (continued)

Signal	Terminal	Signal	Terminal
	Unspecified Data Break Device (continued)		
DI 00	H30D	DI 09	J30D
DI 01	H30E	DI 10	J30E
DI 02	H30H	DI 11	J30H
DI 03	H30K	DI 12	J30K
DI 04	H30M	DI 13	J30M
DI 05	H30P	DI 14	J30P
DI 06	H30S	DI 15	J30S
DI 07	H30T	DI 16	J30T
DI 08	H30V	DI 17	J30V
	H32D	DA 09	J32D
	H32E	DA 10	J32E
	H32H	DA 11	J32H
DA 03	H32K	DA 12	J32K
DA 04	H32M	DA 13	J32M
DA 05	H32P	DA 14	J32P
DA 06	H32S	DA 15	J32S
DA 07	H32T	DA 16	J32T
DA 08	H32V	DA 17	J32V
T5	J28D		
T6	J28E		
DATA RQ	J28H		
DATA IN	J28K		
DATA ACC	J28M		
ADDR ACC	J28P		
DATA RDY	J28S		
DATA SLO RQ	J28T		
	J28V		

The R650 Bus Driver has two types of outputs: fast and slow (or ramp). Using fast output, the bus driver operates as a fast amplifier. When ramp output is used, an integrating capacitor is inserted between the input of the bus driver and the output stage, causing the output lines to move from ground to −3v (or reverse) in approximately 800 nsec. This connection, desirable to reduce crosstalk between lines, is used on the ACB (buffered accumulator) lines.

The W640 Pulse Amplifier modules should be carefully terminated. If sufficient noise is generated at the output of these modules, regeneration may result. For this reason, it is recommended that output lines of W640 Pulse Amplifier modules be well shielded. The outputs of W640 modules may be either 400 nsec or 1 μsec in width. All connections on the standard PDP-7 use the 400 nsec pulse width.

All input signals to the PDP-7 are received by diode gates or inverters. Diode gate inputs draw 1 ma of current from the driving circuit, shared among all inputs at ground potential. Inverter inputs draw 2 ma when the signal is at −3v and provide no load when the signal is at ground potential.

Timing is, in general, determined by the machine itself. However, the following timing considerations apply to the modules. The R111 Diode Gate sets up in approximately 50 nsec in either direction under normal load conditions.

The DCD gates set up in 400 nsec, from the end of the preceding 100-nsec pulse; and the pulse input must return to −3v for 400 nsec before the next pulse is applied. Series R pulses are 100 nsec in width, measured from the 90% point of the leading edge to the 10% point of the trailing edge. Fall time is not critical on these pulses, provided that the pulse has returned to −3v in time to come up for the next cycle.

All output signals from the PDP-7, routed through the interface, have been provided with adequate buffering to meet the input requirements of normal I/O equipment. Whenever it becomes necessary for the user to draw out other signals (besides those connected in the standard interface), care must be taken that the input loads presented to the sources of these signals do not exceed their driving ability. When it is evident that the source would be overloaded, a suitable driver must be provided between the signal source and the I/O device employing the signal.

Device Selector

The DS generates IOT pulses that control I/O equipment and effect information transfers between the computer and peripheral devices. The DS contains a section for standard devices (program interrupt control, real time clock interrupt control, tape reader, tape punch, Teletype units, and display equipment;

or device select codes 00 through 07), and a section for optional equipment (used to expand the DS for all other select codes). Each channel of the optional DS consists of a Type W103 Device Selector module and a W640 Pulse Amplifier module.

Complementary output signals from bits 6-11 of the IOT instruction in the MB are distributed to all channels of the optional DS. These six bits serve as a device select code. The 1 or 0 signal from each MB bit is wired or disconnected in each W103 module to enable a gate only when a pre-established select code occurs in the IOT instruction. When enabled by the correct select code, the W103 module reproduces any IOP pulses as complementary IOT command pulses. Positive IOT pulses are buffered by a circuit of a W640 module before being transmitted over long cables to peripheral devices. These pulses are used in I/O devices for functions such as clearing flags, gating data, setting operation modes, etc. The last digit of any IOT pulse designation corresponds to the number of the IOP pulse which causes generation of that IOT pulse (e.g., combination of a device code XX with an IOP4 pulse produces an IOT XX04 pulse). IOT select code assignments are given in Table 4.

Pulse outputs of the W103 Device Selector module are 100-nsec or 400-nsec collector outputs and can drive any standard R-series FLIP CHIP module located in the proximity of the I/O package. However, most options are located at some distance and require signal transmission over relatively long cables. The W640 Pulse Amplifier modules are capable of driving cables and are wired into appropriate locations to transmit IOT pulses to external devices. The W640 produces 400-nsec pulses (or 1-μsec pulses when appropriate terminals are connected together).

Information Collector

The IC reads data or status information into the AC from various devices. Seven IC channels or levels are available in the basic machines. Each of these channels is wired to a signal cable connector corresponding to an upper half (bits 0-8) and a lower half (bits 9-17) of the AC for optional equipment, or is wired directly to controls for the standard PDP-7 I/O equipment. On the basic machine, the paper-tape reader occupies one complete channel, the Teletype occupies the lower half of a channel, and the status register occupies (nominally) one channel. If no card reader, card punch, or line printer is connected to the system, the lower half of the status register channel may be used for other purposes. Thus, in the basic machine, the equivalent of five free channels is available for additional IC inputs. Channel availability of the IC is specified as follows:

TABLE 4 IOT CODE ASSIGNMENTS

00 1 RT Clock 2 Prog. Interrupt 4 RT Clock	10 Symbol Generator Type 33	20 Memory Increment Type 197	30	40	50	60 Serial Drum Type 24	70 Auto Magnetic Tape Control Type 57A
01 Standard Perforated Tape Reader and Control	11 Analog-to-Digital or Digital-to-Analog Converters	21 Relay Buffer Type 140	31	41	51	61 Serial Drum Type 24	71 Tape Control Type 57A
02 Standard Perforated Tape Punch	12 A-D-A	22 Inter-Processor Buffer Type 195	32	42	52	62 Serial Drum Type 24	72 Tape Control Type 57A
03 1 Keyboard 2 Keyboard 4 IORS	13 A-D-A Stimulus Flag	23 Inter-Processor Buffer Type 195	33 1 33 KSR Skip 2 Clear All Flags 4 Open	43	53	63	73 Tape Control Type 57A
04 Teleprinter	14	24 Incremental Plotter Control Type 350	34	44	54	64	74 Tape Control Type 57A
05 Displays Types 34F, 30D, or 340	15	25 Plotter	35	45	55 Automatic Priority Interrupt Type 172	65 Automatic Line Printer Type 647	75 DECtape Control Type 550
06 Displays	16	26 Plotter	36	46	56 API Type 172	66 Automatic Line Printer Type 647	76 DECtape Control Type 550
07 Display and Light Pen	17 Boundary Register Type KA70A	27 Memory Parity Type 176	37	47	57	67 Card Reader Type CR 01B or Type CR 02A	77 Memory Extension Type 148B

Level	Use
1	All 18 connections employed for RB of the tape reader.
2	First 9 connections employed for status signals of IORS instruction (IOT 0314), and last 6 connections are assigned to the step counter (SC) of the Type 177 EAE option, when present.
3-5	All 18 connections open and assignable.
6	First 10 connections are open and last 8 connections are assigned to Teletype unit.
7	First 12 connections open and assignable.

Each level or channel of the IC consists of one 2-input negative AND gate for each of the 18 possible bits of an input word. The two inputs are usually supplied by a data signal and an IOT pulse which is common to each bit of the input word. Outputs from the seven channels for each bit are NOR combined to set the appropriate accumulator flip-flop. One bit for each of the seven channels is provided by a Type R141 Diode Gate module; the entire IC is constructed of 18 of these modules.

When designing a PDP-7 system, it is necessary to consider the number of IC channels required by peripheral equipment. If more than seven channels are required, the IC must be expanded to accommodate the additional information. Expansion requires a Type 175 Information Collector Expander consisting of 18 Type R141 Diode Gate modules, 6 Type W640 Pulse Amplifier modules, and the appropriate mounting panel and hardware. The Type 175 option connects into the standard IC through two signal cable connectors reserved for this purpose, and adds seven additional information channels. Figure 28 represents the channel assignments for the standard IC.

Information Distributor

Data in the AC is available at the ID of the computer interface as static levels. IOT pulses from the DS can strobe these static levels into an I/O device register. The static level of each ACB output signal is −3v when the bit is a binary 0 or is at ground potential when the bit is a binary 1.

The binary 1 output of each AC flip-flop is power amplified by a Type R650 Bus Driver module in the processor and is applied to the ID for distribution to output devices. These modules have terminals H and S connected to ground so that the output signals have a rise time of approximately 800 nsec. (Without these terminals grounded the rise time is about 50 nsec.) Each R650 output delivers about 20 ma to ground.

The ID provides a series of nine output channels for connection to external devices for the buffered AC signals in locations 13-21 of rows H and J of the I/O package. The prewired connections of the ID to the interface cable receptacles are listed in Table 3.

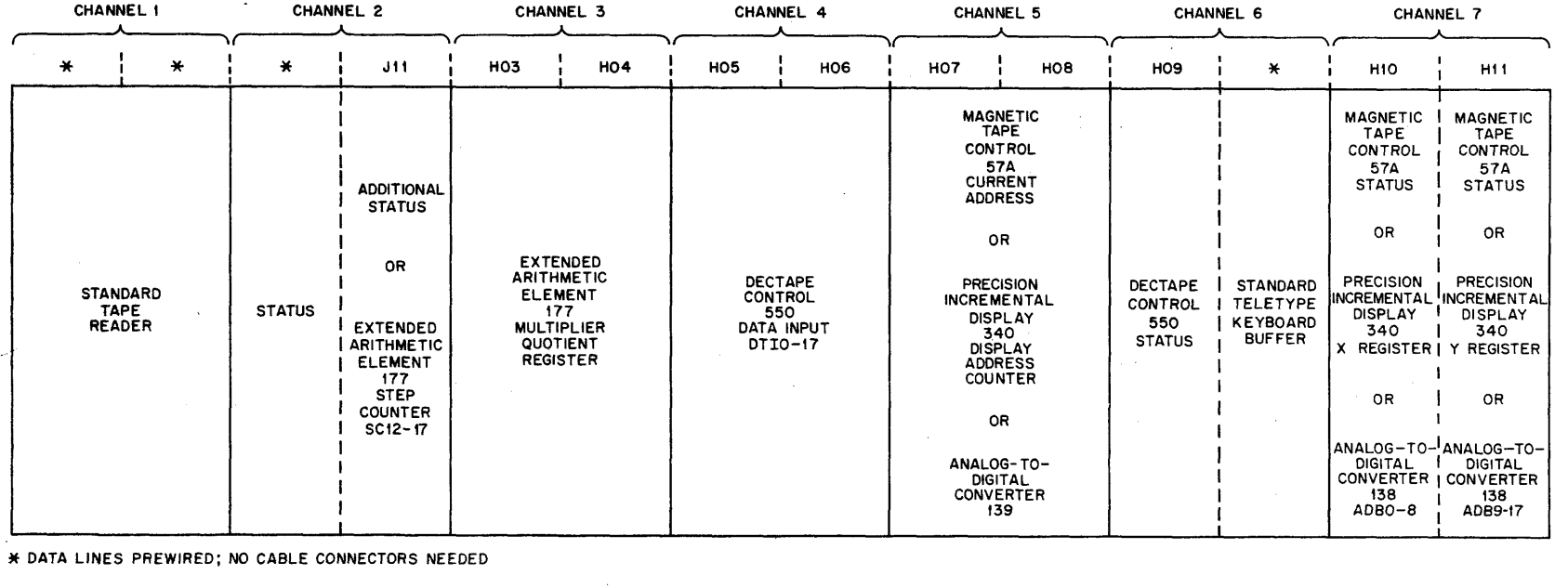


Figure 28 Information Collector Channel Assignments

Power Clear Output Signals

The PWR CLR POS and PWR CLR NEG pulses generate in the I/O package during the first 5-sec interval following setting of the POWER switch to the on position. These pulses initialize and clear processor registers and controls during the power turnon period, and are available to perform similar functions in external equipment. The PWR CLR POS signal is a 375-kc, 100-nsec positive pulse generated in the Type R401 Clock module at location C15. The PWR CLR NEG signal is a 400-nsec negative pulse produced in a pulse amplifier of the Type W640 module at location C13 that is triggered by the PWR CLR POS pulses.

Begin Buffered Output Signal

The BGN (B) signal is supplied to external equipment through a connection in the I/O package interface. This signal is a 400-nsec, −3v pulse generated by a W640 Pulse Amplifier at location C13 of the I/O package during timing pulse SP1•CONTINUE NOT. In I/O equipment, the signal clears registers and resets control flip-flops to initial conditions when the START key on the PDP-7 operator console is operated.

Run Output Signal

The 1 output of the RUN flip-flop is supplied to external equipment through the interface circuits. This RUN (1) signal is at −3v when the computer is performing instructions and is at ground potential when the program is halted. Magnetic tape and DECtape equipment use this signal to stop transport motion when the PDP-7 halts, preventing the tape from running off the end of the reel.

Slow Cycle Request Input Signal

The device selector supplies the SLOW CYCLE REQUEST ground level signal to request that all IOT instructions which address a specific device be executed in a computer slow cycle. This signal is added at the time a slow I/O device is added to the computer system. IOT instructions for the device are decoded in a Type W103 Device Selector module. The ground level output at terminal BD when the device is selected requests the slow cycle by connection to the input of a Type B171 Diode Gate module. This latter module is used as a ground level NOR gate for all such request signals, and a negative output on terminal D of this module is applied to the processor timing circuits. The Type B171 module which receives the SLOW CYCLE REQUEST signals from various devices is located at E14 of the I/O package.

Program Interrupt Request Input Signal

The flag of an external device can request a program interrupt. When the device requires servicing, the condition of the flag, connected to the Type B124 Inverter module in location D27 of the I/O package,

can request a program break. (The flag of the external device should also be connected to the I/O skip facility so that the interrupt program can sense the IOT 01 pulse to determine the device requesting the program break.) The PROGRAM INTERRUPT signal level is the NOR of requests from up to nine devices that require programmed attention. The program interrupt facility can be expanded to accommodate requests from nine additional devices by inserting another Type B124 module in location D28 of the I/O package. When the program break is entered, a subroutine is initiated to determine which device, of many, is to be serviced, and then to perform the appropriate service operation (usually by supplying or receiving data under program control).

Data Break Request Input Signal

A high-speed I/O device may originate a data break request by placing a −3v DATA RQ level on the request line connecting the device to the computer. In the interrupt control, the DATA RQ level is synchronized with delayed timing pulse T5 (T5-DLY) of the current computer cycle, and sets the DATA SYNC flip-flop to 1. This causes a BK RQ level to be transmitted to the major state generator. Completion of the current instruction permits the major state generator to enter a break state, producing a (B) level. This (B) level combines with the DATA SYNC level to produce a negative DATA·B level.

An external device connected to the data break facility of the computer supplies a DATA RQ level, a 15-bit core memory address for the transfer, a signal indicating the direction of the transfer as into or out of the computer core memory, and input or output connections to the MB for 18 data bits. The DATA RQ level is sent to the computer at the time the data is ready for a transfer into the PDP-7 or when the data register in the external device is ready to receive information from the PDP-7. This request level must be −3v for assertion, meaning a request for a data break, and drives a transistor base requiring 2 ma of input current.

Transfer Direction Input Signal

This signal, specifying the direction of data transfer for a data break, is received by the computer from the requesting device. Transfer direction is referenced to the computer core memory, not to the device. This signal is a −3v level when the transfer direction is in, or is ground for an out transfer. A 3-input NAND diode gate for negative levels receives this signal at terminal N18F. The gate also receives the internally generated DATA·B level and T3 pulse to cause generation of the DATA ACC pulse which strobes the DI lines into the MB.

Data Address Input Signal

During an ADDR ACC pulse of a break cycle, the data address given by an I/O device is transferred to the MA by connections made at the DA level input of a NOR gate in each module of the MA.

Address Accepted Output Signal

At time T1 of the break cycle, the DATA•B level NAND combines with timing pulse T1 to produce an ADDR ACC pulse (called DATA ADDR ⟶ MA pulse in early systems). This pulse transfers the memory address in the address register of the I/O device into the processor MA. This pulse also acknowledges to the external device that its address has been accepted.

Data Information Input Signals

The 18 DI lines establish the data to be transferred into the MB from an external device during a data break in which the direction of transfer is into the PDP-7. The DI signal levels, presented to 2-input negative NAND diode gates at the binary 1 input of the MB, are transferred into the MB by the DATA ACC pulse. This information in the MB is then written into core memory during a normal write operation. The DI signals are −3v to designate a binary 1 or ground potential to specify a binary 0, and should be available at the time the break request is made.

Data Accepted Output Signal

During time T3 of a data break cycle, when the external device requests a transfer into the PDP-7, the DATA•B level causes a negative DATA ACC pulse (called DATA INFO ⟶ MB in early systems) to be generated. This pulse strobes the data input gates of the MB to transfer a data word from an external device into the MB. This pulse is also an output for device synchronization. Starting at time T5, information in the MB is written into core memory by the normal write operation.

Data Ready Output Signal

During T3 of a data break cycle in which the transfer direction is out, the DATA·B level causes a negative DATA RDY (in early systems called MB INFO ⟶ OUT) pulse to be generated. This pulse may strobe MBB information into the external device buffer; for this purpose the signal may be delayed within the device to strobe the data into the buffer after an appropriate setup time. Note that the transfer must occur prior to T2 of the next computer cycle.

Data Information Output Signals

Data break transfer from core memory to an I/O device is made through the MB, whose output is buffered for this purpose by 18 Type B684 Bus Drivers. Each bus driver is capable of driving a 40-ma load. The MBB output terminals are in the I/O package.

CHAPTER 6

INSTALLATION PLANNING

PHYSICAL CONFIGURATION

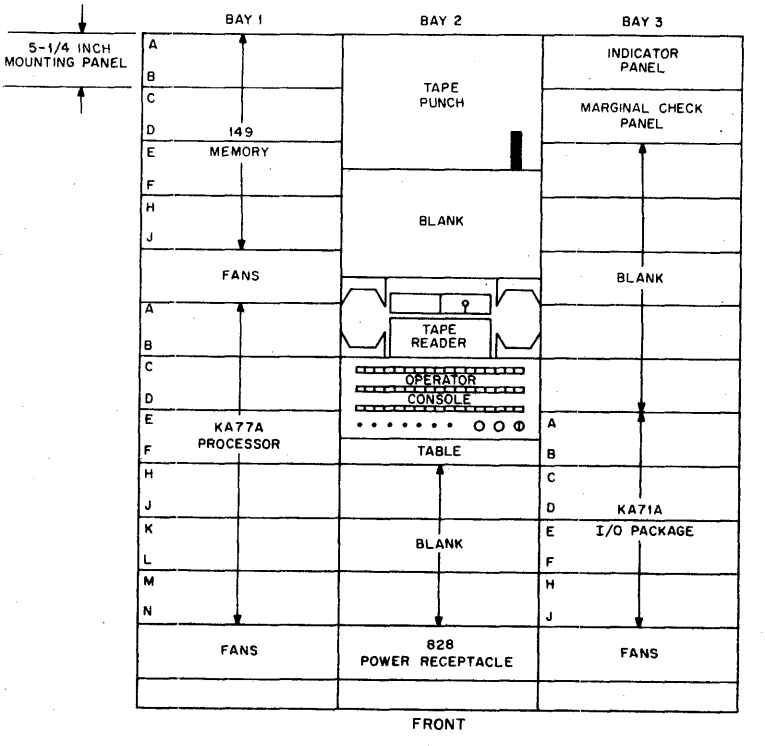
The basic PDP-7 is housed in a three-bay cabinet and consists essentially of mounting panels of FLIP CHIP modules. Figure 29 shows the physical location of the memory, processor, I/O package, operator console, tape reader, and tape punch within the basic system. Space is available for optional equipment below the table in the center bay and above the I/O package in the right bay. For example, a three-bay PDP-7 with 8192 words of core memory could also include an Automatic Priority Interrupt Type 172B and have space for analog-to-digital or CRT display options. Larger systems are constructed by adding standard computer bays to either or both sides of the basic machine and/or in free-standing cabinets. Memory options above 8K mount in bays to the left of the processor and additional I/O options mount to the right of the I/O package. The location of many options is fixed for technical reasons. For example the Extended Arithmetic Element Type 177B mounts above the Power Receptacle Type 828 in the center bay of the basic machine. Preferred locations for most options are shown in Figure 30.

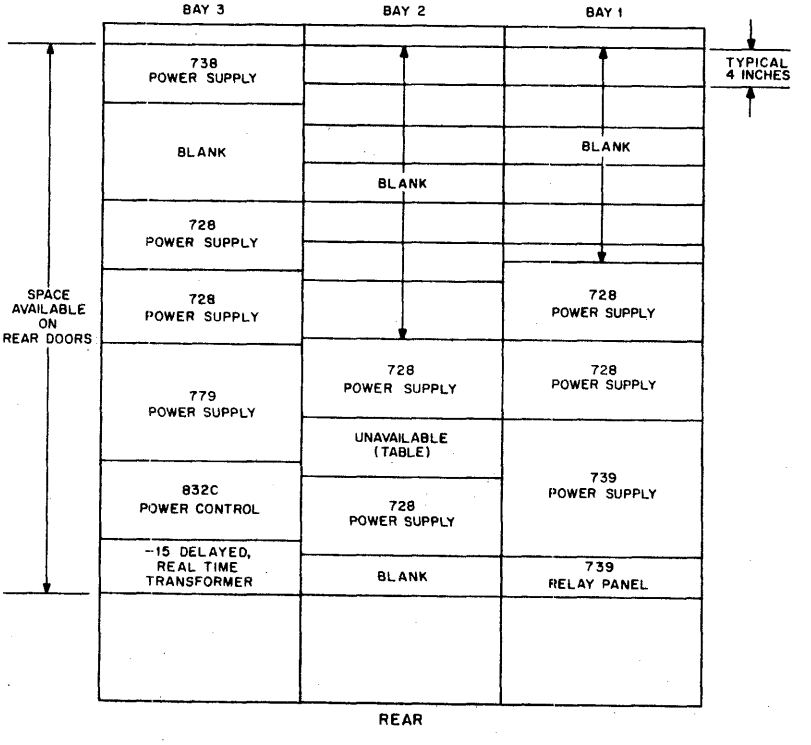
Each standard DEC cabinet bay can accommodate twelve module mounting panels. However, the top and bottom locations are reserved for indicator panels, fans, etc., and should not be used to mount logic circuits. Standard cabinet bays are joined by removing end panels and bolting the frames together. Overall dimensions are then reduced by the width of the removed end panel (1-1/4 inches per side); weight is reduced 45 pounds per end panel. Access to all logic wiring is from the console side of the computer. All cabinet bays are mounted on four heavy-duty casters. The floor plan for the basic PDP-7 shown in Figure 31 can be used for installation planning.

Table 5 summarizes physical and electrical data for the basic PDP-7 and for most optional equipment. The number of cabinet bays required for a particular installation can be determined from this table.

ENVIRONMENTAL REQUIREMENTS

The PDP-7 processor and input/output devices operate satisfactorily under ordinary conditions of humidity, shock, and vibration in a 50° to 122°F temperature range. However, a 70° to 85°F temperature range and a 30 to 80% humidity range are recommended. Consult the system heat characteristics listed in Table 5 if room air-conditioning is planned.

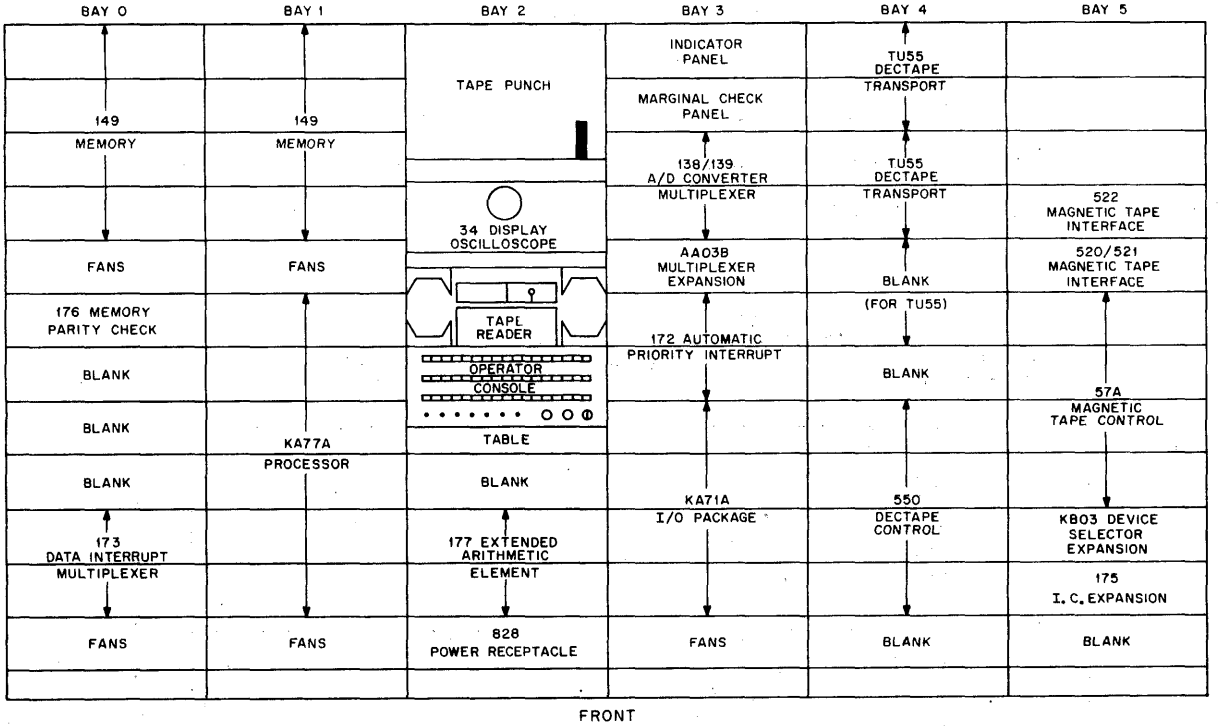




REAR SPACE REQUIREMENTS

EQUIPMENT TYPE	VERTICLE SPACE REQ'D
728A POWER SUPPLY	8 INCHES
734A,B,C POWER SUPPLY	8 INCHES
743A POWER SUPPLY	12 INCHES
772A POWER SUPPLY	8 INCHES
778A POWER SUPPLY	12 INCHES
779A POWER SUPPLY	12 INCHES
832 POWER CONTROL	8 INCHES

Figure 29 Basic PDP-7 Component Locations



NOTE:
IF 522 INTERFACE IS USED, TWO
MOUNTING PANELS ARE REQUIRED

Figure 30 Typical PDP-7 System Component Locations

POWER REQUIREMENTS

The PDP-7 requires a source of 115v, 60-cps, single-phase power. On special request, all equipment can be factory wired for 50-cps and/or 220 to 250v power. The power source must maintain the nominal voltage within ±10% under normal and transient load conditions. The electrical characteristics of individual units are given in Table 5.

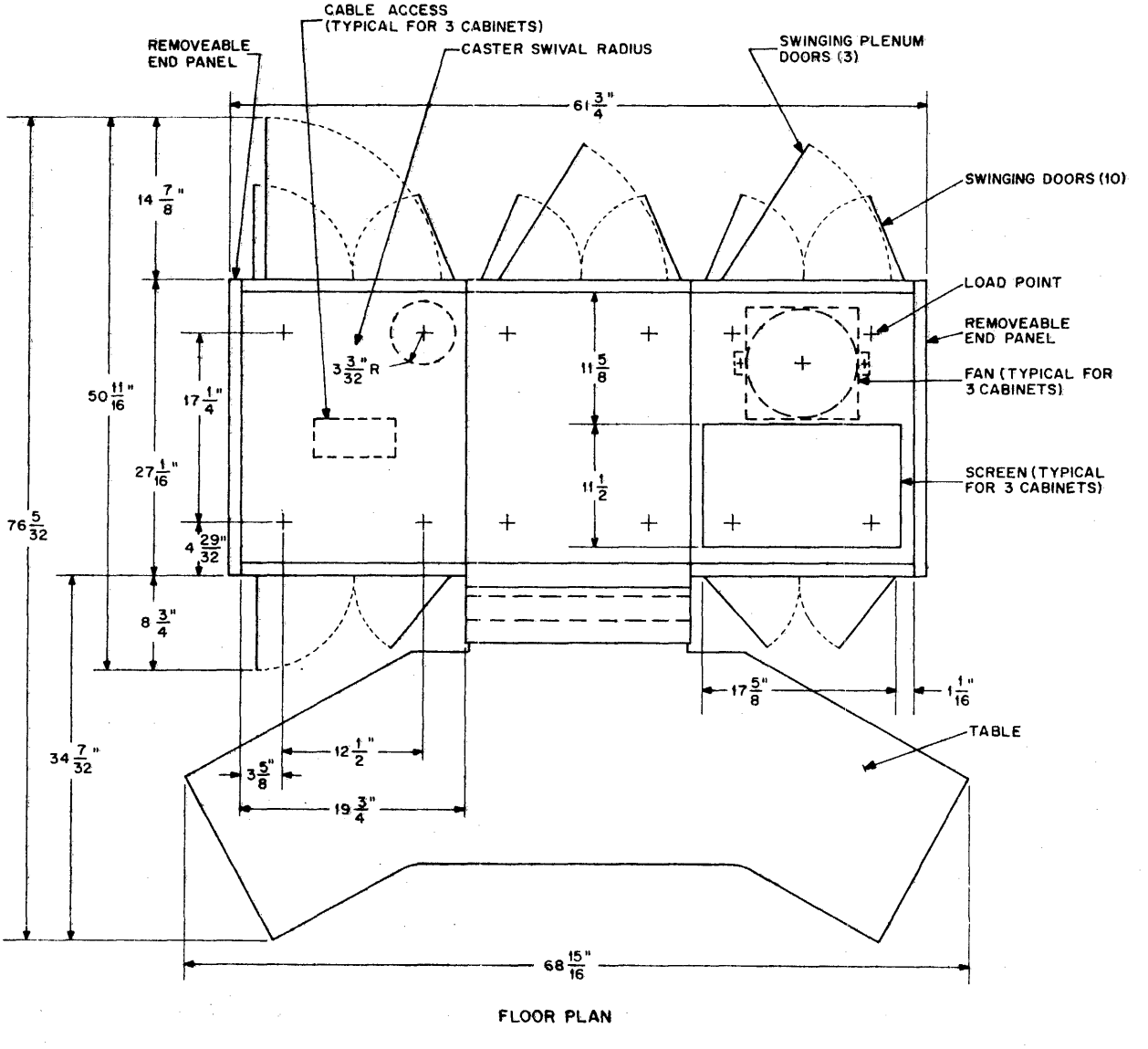


Figure 31 Basic PDP-7 Installation Dimensions

CABLING REQUIREMENTS

All system power sources should have 115v, 30-amp, Hubbel Twistlock flush receptacles (or their equivalent) to mate with equipment power cables.

TABLE 5 INSTALLATION DATA *

	Dimensions (inches)			Panels	Cabinets	Weight (lbs.)	Service Clearance Required (inches)		Current (Amps)		Heat Dissipation (BTU/hr)	Power Dissipation (KW)
	Height	Width	Depth (incl. tables)				Front	Rear	Nominal	Surge		
Standard PDP-7	69-1/8	61-3/4	61-1/4	36	3	1150	8-3/4	14-7/8	17	30	7150	2.1
Core Memory Module 147	--	--	--	--	--	5	--	--	--	--	--	--
Memory Extension Control 148B**	--	--	--	--	--	--	--	--	0.5	7.5	204	0.06
Core Memory Module 149A	--	--	--	4	--	80	--	--	5.5	7.5	2040	0.6
Priority Interrupt 172B	--	--	--	2	--	60	--	--	1.5	2.75	612	0.18
Data Interrupt Multiplexer 173	--	--	--	2	--	40	--	--	1	2	408	0.12
Extended Arithmetic Element 177B	--	--	--	--	--	40	--	--	1	2	408	0.12
Dual DECtape Transport 555	12	19	17-1/2	--	--	65	2-1/4	--	1.5	3.2	585	0.172
DECtape Control 550	--	--	--	4	--	255	8-3/4	14-7/8	1.5	3.2	585	0.172
Magnetic Tape Transport 50	69-1/8	22-1/4	27-1/16	--	1	600	18-5/16	14-7/8	8	12	2114	0.62
Automatic Magnetic Tape Control 57A	--	--	--	5	--	281	8-3/4	14-7/8	4	6	1564	0.460
Magnetic Tape Transport 570	68	32-1/8	32-3/8	--	1	850	30	14-7/8	25	38	9800	2.9
Magnetic Tape Transport 545	69-1/8	22-1/4	27-1/16	--	1	400	18-5/8	14-7/8	8	12	2114	0.62
Serial Drum 24	69-1/8	22-1/4	27-1/16	--	1	500	9	15	5	8	1540	0.45
Oscilloscope Display 34F**	--	--	--	--	--	--	--	--	1	2	408	0.12
CRT Display 340	69-1/8	42	51	1	2	700	8-3/4	36	15	20	5900	1.73
Slave Display 343	69-1/8	22-1/4	51	--	1	350	8-3/4	36	6	10	2350	0.69
18-Bit Relay Buffer 140	--	--	--	2	--	40	--	--	1	2	408	0.12
A-D Converter 138E; 64Channel Multiplexer Control 139E	--	--	--	3	--	50	--	--	0.6	0.77	612	0.18
Data Communication System 630 (8 line)	--	--	--	2	--	40	--	--	1	2	4080	1.2
Automatic Line Printer and Control 647	52-57	56	30-1/4	--	1	1350	24	26	13	19	5304	1.56
Card Reader and Control CR01B (100 cpm)	8-1/4	18	10	--	1	25	--	6-5/8	0.57	1	204	0.06
Typical Standard Cabinet Bay (empty)	69-1/8	22-1/4	27-1/16	12	1	100	8-3/4	14-7/8	--	--	--	--

REMARKS

Standard PDP-7

Third bay has space for five panels of options.

Core Memory Module 147

Fits in first bay of basic PDP-7.

12-16K memory requires minimum four-bay configuration.

Core Memory Module 147 (continued)

20-32K memory requires five-bay configuration.

Draws no extra power.

Extended Arithmetic Element 177B

Fits in second bay of standard PDP-7.

Dual DECtape Transport 555

Provision is made for installation of this unit in bay two of standard PDP-7.

Table model dimensions are given. Also can be mounted in two mounting panel positions.

DECtape Control 550

Mounted in standard bay.

Magnetic Tape Transport 570

Nonstandard cabinet.

Oscilloscope Display 34F

Space for control logic is provided in basic I/O package.

Oscilloscope RM503 requires additional panel or may be mounted externally.

Card Reader & Control CR01B

Table top model.

Requires one panel of additional cabinet space.

CRT Display 340

Requires one panel in bay three for cable connection to the external cabinet.

*This information is invalid for PDP-7's with serial numbers below 100.

**Mounted within basic computer

Nineteen-wire ribbon cables with Type W021 Cable Connectors provide signal connection between the computer and optional equipment in the basic computer cabinets or in cabinets bolted to the basic computer bays. These cables are connected by plugging the W021 Connectors into standard FLIP CHIP module receptacles.

Fifty-wire shielded signal cables with Amphenol 115-114P male connectors at both ends interconnect the processor and peripheral equipment in separate free-standing cabinets. Any special equipment using these cables must have Amphenol 115-114S female connectors and 1391 shells to accept signal cables.

Unless otherwise specified, power cables are supplied in 25 ft lengths, permanently wired at one end to individual units. Signal cables come unattached in 25 ft lengths. Power and 50-pin signal cables measure 11/16 and 13/16 inch in diameter, respectively.

All free-standing cabinets require independent 115v receptacles. However, these units may be turned on or off or controlled from the PDP-7 console.

Cables are connected to cabinets through a drop panel in the bottom of cabinets. Subflooring is not necessary because cabinets are elevated from the floor by casters to afford sufficient cable clearance.

APPENDIX 1

PDP-7 DEVICE SELECTOR AND INFORMATION COLLECTOR REQUIREMENTS FOR STANDARD OPTIONS

The standard device selector on a PDP-7 with a tape reader, tape punch, and Teletype contains 12 spare selector channels. Each selector channel in a PDP-7 with a serial number over 100 requires a W103 Device Selector module and a W640 Pulse Amplifier module (three circuits producing 400-nsec or 1-μsec pulses).

The standard information collector on a PDP-7 with a tape reader, tape punch, and Teletype contains 5 spare input channels. One Type 175 Information Collector Expansion option extends the standard IC by seven additional channels, making a total of 12 available channels. The 175 requires one channel of the standard IC; the total number of available channels is 11.

The following list specifies the number of DS and IC channels required for standard DEC options for the PDP-7. By using the following list, the need for DS or IC expansion can easily be determined for any system configuration containing standard DEC options. If required, these expansion elements should be included in purchase orders and construction requisitions. In cases where only half a channel is required, the remaining half is available for other options. Half channels are designated as 0.5L for the left half (bits 0 through 8) or 0.5R for the right half (bits 9 through 17).

Option	DS Channels	IC Channels
Second Console Teletype and Control 649B	2	1
Memory Extension Control 148B	1	0
Memory Parity 176	1	0
Memory Increment 197	1	1
Memory Boundary Register KA70A	0	0
Automatic Priority Interrupt 172B	2	0
Data Interrupt Multiplexer 173	0	0
Extended Arithmetic Element 177B	0	1.5R
DECtape Control 550	2	1.5L
Automatic Magnetic Tape Control 57A	5	2
Serial Drum 24	3	0
Incremental Plotter and Control 350	3	0

Option	DS Channels	IC Channels
Oscilloscope Display 34F	2	0
Precision CRT Display 30D	3	0
Symbol Generator 33 (for 30D)	1	0
Precision Incremental Display 340	4	2
Subroutine Option 347 (for 340)	4	4
Character Generator 342 (for 340)	0	0
Slave Display 343 (for 340)	0	0
Photomultiplier Light Pen 370	1	0
Relay Buffer 140	1	0
Analog-to-Digital Converter 138E	1	1
General Purpose Multiplexer 139E	2	0.5R
Digital-to-Analog Converter AA01A	3	0
Data Communications System 630	62	0.5R
Automatic Line Printer 647	2	0
Card Reader and Control CR01B	1	1
Card Reader and Control CR02A	1	1
Interprocessor Buffer 195	2	1

digital
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